Wafer Foundry Services

408-432-9100 www.impweb.com info@impinc.com

- Service Overview
- Selection Guide
- Process Specifications
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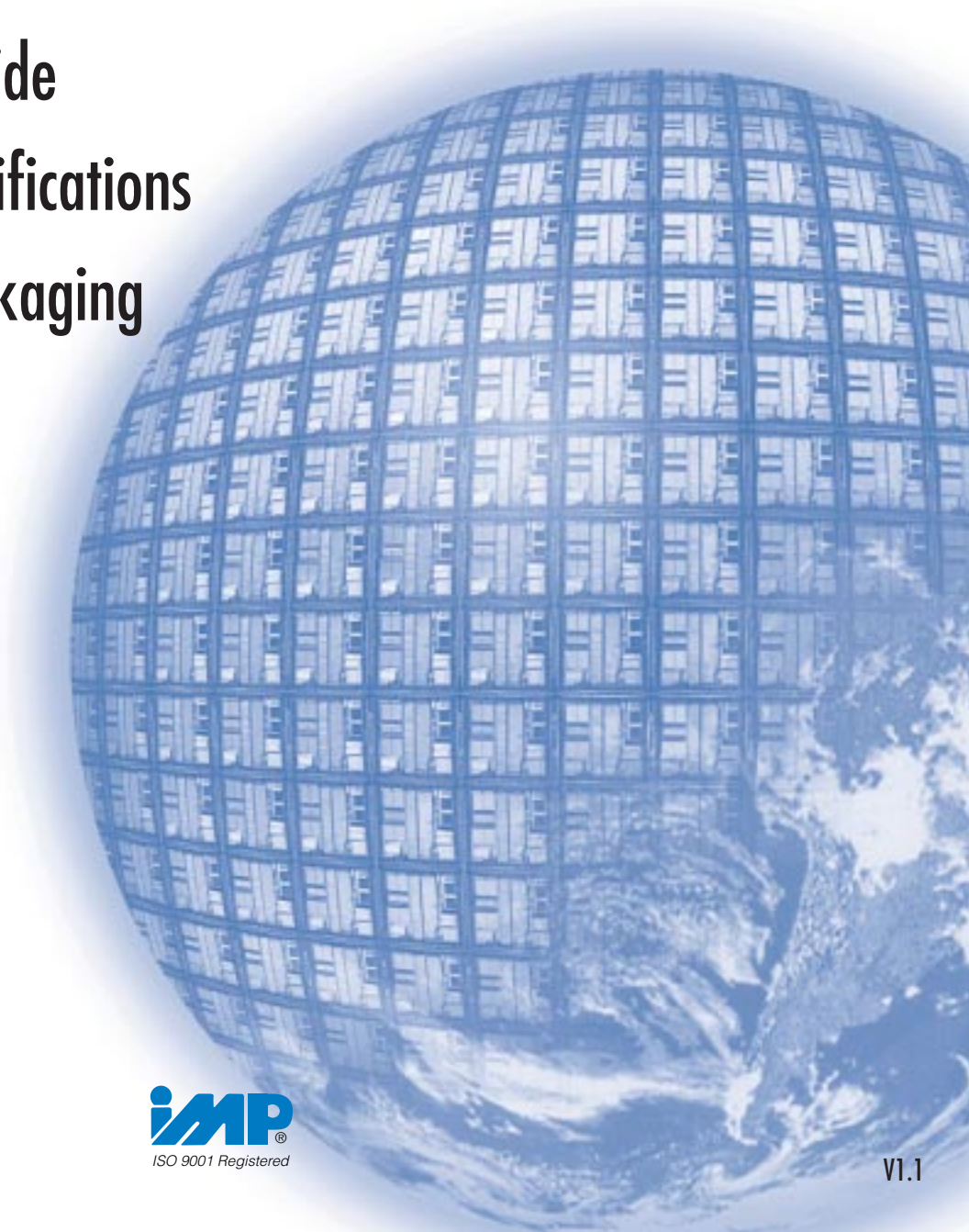
- Quality



ISO 9001 Registered

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Introduction to Wafer Fabrication Services

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Customer Centered Silicon Wafer Fabrication Services

Introduction

IMP specializes in high-volume manufacturing of analog and mixed-signal process technologies. Standard analog and mixed-signal capabilities include low (1.5V) and high voltage (12/20/30/100V) processes, low temperature coefficient poly resistors, Schottky diodes, fusible link technology, EPROM/EEPROM modules, high resistivity poly and double poly process options. IMP also has volume manufacturing expertise in processes above 500 Volts.

A particular strength of IMP is the ability to rapidly port a customer's existing process into the volume production facility.

IMP participates in four business areas:

- **Database Production**
  Customer products designed for standard IMP processes and design rules.
- **Process Porting**
  Customer developed wafer manufacturing processes are installed in IMP facilities.
- **Process Development**
  Major modification to an existing IMP process to meet specific customer requirements.
- **Silicon Venture Partner**
  Project partnerships with fabless start-ups.

IMP will supply customers with wafers, die or finished packaged and tested devices.

Domestic Wafer Fabrication Facility

IMP operates an ISO 9001 registered, 16,000 square foot facility in San Jose, CA, with an 8,000 square foot class 10 clean room. Wafer capacity is 20,000, 5" wafers starts per month.

With a USA based location, domestic customers receive same-day, real-time answers to technical and delivery queries. Compared to Pacific Rim and European foundries, communication with IMP is easy, faster and more economical. A fast, effective communication channel is an often overlooked key factor in selecting a foundry partner.

Flexibility

Tight design rules and a staff of experienced process technologists allow IMP to accommodate almost any customer requirement. Unlike many foundries with rigid "canned" options, IMP actively encourages partners with new or modified process requirements. An existing process can be ported to IMP's facility when volume warrants.

IMP will supply wafers, die or provide a complete turn key solution

IMP Custom Silicon Support Teams

To meet the rapidly changing needs of our customers, we provide a highly flexible and responsive service. To that end, our engineering staff works closely with you from the difficult phase of prototyping through to full circuit production.

Our silicon foundry operation centers around technical account managers, dedicated production planning administrators, and process and circuit designers operating as a consulting team for the customer.

Experienced in the design, fabrication, packaging and testing of digital, analog, and mixed-signal integrated circuits, these experts are available at any time to meet with your technical and business staff to assist in delivering high quality prototype and production wafers to your schedule and at the highest quality levels. The staff will work with foundry partners to enhance yield and advise on changes that will improve manufacturability.

Our commitment to this level of customer support is because we recognize its importance in achieving timely product introductions in highly competitive markets.

Design Inputs

The IMP wafer foundry accepts customer database designs in GDS II format and PG tapes. If required engineering support is available to convert your tooling from an existing foundry to IMP standards. IMP provides all the design rules and electrical parameters needed to modify new designs.

Test Capability

IMP offers a full range of test capability for digital, analog and mixed-signal products. Precision analog and high speed mixed-signal capability is available.

IMP has in-house test capability for both digital and analog tests using Trillium, Sentry 20/21, LTX77/ Synchro, MCT and other testers.

Packaging

IMP recognizes time-to-market is a critical customer concern and that fast turnaround prototypes are a key element in reducing a foundry partner's time-to-market. IMP operates an in-house prototype packaging service for fast response.

High-volume production packaging services are provided by IMP qualified assembly vendors.

Delivering Quality

IMP Facilities are certified to ISO 9001, 1994 Edition. In 1996, IMP received dual certification by the American National Standards Institute Registration Board (RAB) in the U.S. and by the Dutch Council for Accreditation (RvA) in Europe.

IMP uses statistical process control for real time monitoring of all silicon manufacturing operations. Over 180 control charts are maintained on-line. Cp and Cpk trends are maintained on critical parameters such as: gate oxide thickness, poly sheet resistance, poly width, diffusion width, field oxide thickness, intermetal oxide thickness, threshold voltages, breakdown voltages and transistor gains. Device parameters are collected on all processes. The result is exceptional quality.

Many leading companies have selected IMP as their manufacturing partner:

- Adaptec
- Apple Computer
- Conner Archive
- Hewlett Packard
- International Rectifier
- Level One
- Linfinity
- Rockwell International
- Siemens
- Tektronix
- TEMIC

Turnkey Solutions

Customers with turn-key requirements are served with IMP's production-proven test facility, quick-turn in-house packaging capability and off-shore volume packaging resources.

Packaged devices can be drop shipped to customers anywhere in the world.

Intellectual Property Security

All customer designs and tooling are held in the strictest confidence.

Your Next Step

The IMP team approach to silicon foundry services is your path to satisfaction. Whether you have your own design resource and facility, want to utilize outside third-party design expertise, want to port an existing process or need a process designed to your specification or are simply seeking a second source, IMP is the foundry to provide you with cost-effective and timely silicon solutions.

Company Profile

IMP, Inc. designs, manufactures and markets standard-setting analog integrated circuits and specialty analog wafer foundry processes for data communications and power management applications in computer, communications and control systems. IMP products are sold through a worldwide network of representatives and distributors

Company Facilities

IMP headquarters and ISO 9001 certified wafer fabrication and test facility are located in San Jose, California. Product development centers are in Pleasanton, California and Lee, New Hampshire. The company employs 225 people.

Wafer Fabrication and Manufacturing Services

High-volume, analog and mixed-signal wafer foundry services on low-power, high-voltage, CMOS, BiCMOS, and EEPROM processes, including turnkey packaging and test capabilities. Fabrication services include database production using IMP standard processes, and porting of customer-owned technology.

Analog Integrated Circuit Products

Innovative analog integrated circuit products serving basic system infrastructure applications in computer, communications and control systems. Key areas of focus are;

Data Communications Interface - Internal system data communications devices, including memory bus terminators and second-generation Small Computer Serial Interface (SCSI) terminators.

Power Management - Devices to generate, distribute, protect and manage thermal and power consumption characteristics of desktop and portable computers, mobile communication devices and battery powered electronic systems. Examples include microprocessor supervisors and high-frequency switching converters.

The company also supplies read-channels, preamplifiers, programmable filters, write drivers and other complex mixed-signal ICs for tape back-up and other mass-storage peripherals.

Management

Phil Ferguson, President and CEO; Tarsaim Batra, VP manufacturing; Jerry DaBell, Senior VP product development; Moiz Khambaty, VP technology; Ron Laugesen, VP product and test engineering; and Barry Wiley, VP marketing and sales.

Board members are Phil Ferguson, President and CEO; Zvi Grinfas, Consultant; Peter D. Olson, President and CEO of H3D, Inc.; and Bernard V. Vonderschmitt, Chairman of Xilinx, Inc.

For More Information

Write, call or fax the company; visit the IMP web site at www.impweb.com; email info@impinc.com or contact the Fax-on-Demand system at 1-800-249-1614 (domestic)/303-575-6156 (international).

Capability and Services

CMOS Technology

IMP offers a wide selection of single/double metal and single/double poly layer CMOS technologies, down to 0.8 micron feature sizes. This includes n-well and p-well versions with epitaxial/non-epitaxial starting materials and custom parameter options for specific applications.

Low and zero threshold process are available. Poly-to-poly capacitors are available for analog signal conditioning applications. Operating voltages range from 1.5V to 100V.

BiCMOS Technology

IMP combines bipolar and CMOS processes into a highly integrated solution for users requiring the speed of bipolar and low power/high density of CMOS. BiCMOS product offerings include 5V, 12V and 30V processes. High sheet resistance poly is available for high-value resistor applications. A low temperature coefficient poly is available for low temperature coefficient (TC) resistors.

High Voltage Technology

A 15V, 1.2 micron process combines the digital density of a 1.2 micron double metal process with high voltage drivers through a dual-gate approach. This combination makes the process attractive for applications such as LCD display drivers, print-head drivers, peripheral interface circuits, motor controllers, PWM/SMPS controllers and CCD drivers which often require large amounts of dense logic on the same chip. The basic design rule set of a 1.2 micron process applies with separate rules for the high-voltage section.

Several 30V BiCMOS processes target power management applications, such as SMPS controllers, traditionally served by bipolar technology.

IMP, 100V process targets SMPS controllers, Electroluminescent (EL) and Vacuum Florecsent (VF) display drivers and computer peripherals.

EEPROM and EPROM Technology

Electrically erasable CMOS technology provides programmability in digital and mixed-signal systems. IMP's EECMOS process simplifies post-fabrication calibrations and reprogramming for custom digital and analog logic applications.

Low Voltage Technology

A true low-voltage process has been developed by enhancing IMP's standard CMOS technology. It is a product of IMP's expertise in mixed analog and digital CMOS process technology and internal circuit design need. This process meets 3V power supply requirements and can be used for 1.5V battery-operated IC products. IMP manufactures integrated disk drive read channel ICs using this production proven 3V process.

Packaging

IMP offers a wide selection of industry-standard packages. Thru-hole packages include dual-inline-packages (DIP) and pin grid arrays. Surface-mount packages, from 3 to 256 pins, include small-outline IC (SOIC) and SOT packages, plastic and ceramic leaded chip carriers, and quad flat packs. Thin surface-mount packages are available in thin quad flat packs (TQFP) and thin small outline packs (TSOPs).

Test

IMP has in-house test capability for both digital, analog and mixed-signal tests using Trillium, Sentry 20/21, LTX77/Synchro, MCT and other testers.

Process Selection Guide and Technology

ISO 9001 Registered

Process Selection Guide

New Offering	Process	Technology (µ)	# Poly Layers	# Metal Layers	# Masks	Well Type	Digital	Analog	BiCMOS	E^2	High Voltage	Low Threshold	High ρ Poly	Low TC Poly Resistors	Schottky Diode	Low-Voltage Bipolar	High-Voltage Bipolar	Low-Voltage CMOS	High-Voltage CMOS	Comments
	C0809	0.8	2	2	14	N		■										5		
◆	C0810	0.8	2	2	15	N		■					■					5		High Density Analog Circuits
	C1004	1.0	1	2	12	N	■											5		Gate Array Applications
	C1012	1.0	1	2	14	N												5		NCR Equivalent
	C1015	1.0	2	2	14	N		■										5		
◆	C1026	1.0	2	2	20	N		■	■		■			■	■	5		5	20	
◆	C1027	1.0	2	2	18	N		■	■		■			■		5		5	20	
◆	C1028	1.0	2	2	20	N		■	■		■			■		5		5	20	
◆	C1029	1.0	2	2	20	N		■	■		■		■		■	5		5	20	
	C1201	1.2	1	2	11	N	■											5		
	C1202	1.2	2	2	12	N		■										5		
	C1203	1.2	2	2	14	N			■							5		5		Low cost 2GHz Process
	C1206	1.2	2	2	16	N			■							5		5		6.4GHz Process
	C1209	1.2	2	2	14	N				■								5		Mixed-Signal Process
	C1210	1.2	2	2	14	N		■				■						5		Zero Threshold Devices
	C1212	1.2	2	2	17	N		■	■								12	5		
	C1215	1.2	2	2	13	N		■				■						5		Low Threshold Devices
	C1216	1.2	2	2	15	N		■			■								15	Under Development
	C1219	1.2	2	2	17	N		■		■		■	■					5		
	C1221	1.2	2	2	18	N		■	■				■			5		5		6.2GHz
	C1225	1.2	1	2	16	N		■	■							5		5		
	C1226	1.2	2	2	19	N		■			■							5	100	
	C1227	1.2	2	2	15	N		■	■		■		■			5			30	
◆	C1229	1.2	2	2	13	N		■			■		■					5	30	
◆	C1230	1.2	2	2	18	N		■	■					■		5		5		
◆	C1231	1.2	2	2	16	N		■	■		■			■		5	30	5	30	
◆	C1232	1.2	2	2	20	N		■	■	■		■	■			5		5		
	C1601	1.6	2	2	13	N		■										5		Mixed-Signal Designs
	C3013	3	2	1	11	P		■										5	10	
	C3014	2	2	1	10	P						■						5	10	
	C3015	3	1	1	9	P	■												10	
	C3017	3	2	2	13	P		■											10	
	C3025	3	2	1	9	P		■											10	
	C5014	5	2	1	11	P		■			■								15	15V RCA/AMI Equivalent

Process Technology Overview

IMP processes cover a wide range of operating voltages from 1.5 Volts up to 100 Volts. All processes are available with double poly and double metal layers.

Process / Parameters Technology	**5.0 Micron** CMOS	**3.0 Micron** CMOS	**1.2 Micron** CMOS BiCMOS EEPROM	**1.2 Micron** High Voltage	**1.0 Micron** CMOS	**0.8 Micron** CMOS
Well Type	Both	P-Well	N-Well	N-Well	N-Well	N-Well
Poly Layers	Single/Double	Single/Double	Single/Double	Single/Double	Single/Double	Single/Double
Poly Width / Space (μm)	5.0/2.5	3.0/2.5	1.5/2.0	1.5/2	1.0/1.4	0.8/1.0
Metal Layers	Single/Double	Single/Double	Single/Double	Single/Double	Single/Double	Single/Double
Metal 1 Width/Space (μm)	5.0/3.0	3.5/2.5	2.5/1.5	2.5/1.5	1.4/1.2	1.4/1.0
Metal 2 Width/Space (μm)	7.0/3.0	5.0/3.0	2.5/1.5	2.5/1.5	2.0/1.4	1.4/1.1
Contact (μm)	3.0x3.0	2.0x2.0	1.5x1.5	1.5x1.5	1.2x1.2	0.8x0.8
Via (μm)	3.0x3.0	2.0x2.0	1.5x1.5	1.5x1.5	1.2x1.2	0.8x0.8
Operating Voltage (V)	15/10	10/5/3	15/5/3	100/5	5/3	5/3
Gate Oxide Thickness (Å)	1,080	500	250	240	210	170
Field Oxide Thickness (Å)	13,000	8,000	8,000	8,000	7,000	4,500
Conduction Factor- N	26	47	75	78	87	95
Conduction Factor- P	9.0	17	25	25	28	31
B_{VDSSN} (min) (V)	20	12	18/7/7	100/5	7	7
B_{VDSSP} (min) (V)	-20	-12	-18/-7/-7	-100/-5	-7	-7
Process	C5014	C3017	C1202	C1226	C1004	C0809

Process C0809
CMOS 0.8µm
5 Volt Analog

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_N	0.6	0.8	1.0	V	100x0.8µm
Body Factor	γ_N		0.74		$V^{1/2}$	100x0.8µm
Conduction Factor	β_N	75	94	115	µA/V^2	100x100µm
Effective Channel Length	$Leff_N$		0.8		µm	100x0.8µm
Width Encroachment	ΔW_N		0.3		µm	Per side
Punch Through Voltage	$BVDSS_N$	7	13		V	
Poly Field Threshold	$VTF_{P(N)}$	10	17		V	

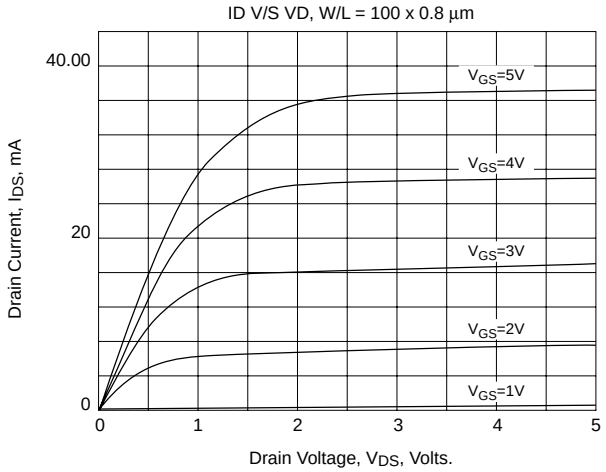
P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_P	–0.7	–0.9	–1.1	V	100x0.8µm
Body Factor	γ_P		0.57		$V^{1/2}$	100x0.8µm
Conduction Factor	β_P	25	31	37	µA/V^2	100x100µm
Effective Channel Length	$Leff_P$		0.85		µm	100x0.8µm
Width Encroachment	ΔW_P		0.4		µm	Per side
Punch Through Voltage	$BVDSS_P$	–7	–12		V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–10	–17		V	

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{N\text{-well(f)}}$	0.50	0.65	0.80	KΩ/□	n-well
N+ Sheet Resistance	ρ_{N+}	45	60	75	Ω/□	
N+ Junction Depth	x_{jN+}		0.25		µm	
P+ Sheet Resistance	ρ_{P+}	68	90	112	Ω/□	
P+ Junction Depth	x_{jP+}		0.4		µm	
Gate Oxide Thickness	T_{GOX}		17.5		nm	
Field Oxide Thickness	T_{FIELD}		700		nm	
Bottom Poly Sheet Res.	ρ_{POLY1}	15	23	32	Ω/□	
Gate Poly Sheet Resistance	ρ_{POLY2}	15	23	32	Ω/□	
Metal-1 Sheet Resistance	ρ_{M1}	40	60	80	mΩ/□	
Metal-2 Sheet Resistance	ρ_{M2}	20	30	40	mΩ/□	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.
High Resistance Poly	$\rho_{HI\text{-}POLY}$	1.5	2.0	2.5	KΩ/□	

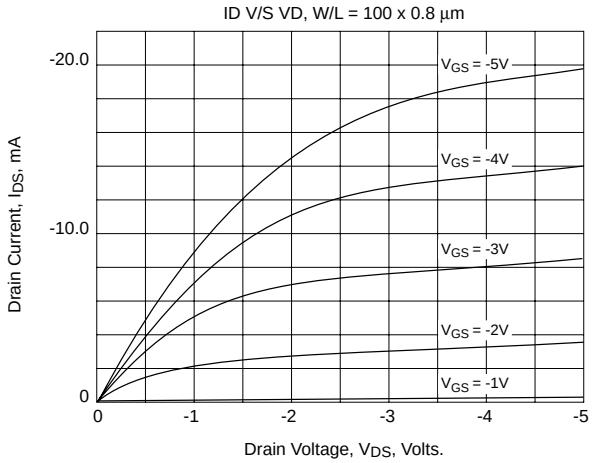
Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}		1.97		fF/µm^2	
Metal-1 to Poly1	C_{M1P}		0.046		fF/µm^2	
Metal-1 to Silicon	C_{M1S}		0.028		fF/µm^2	
Metal-2 to Metal-1	C_{MM}		0.038		fF/µm^2	
Poly-1 to Poly-2	C_{PP}	0.69	0.822	1.015	fF/µm^2	

Physical Characteristics

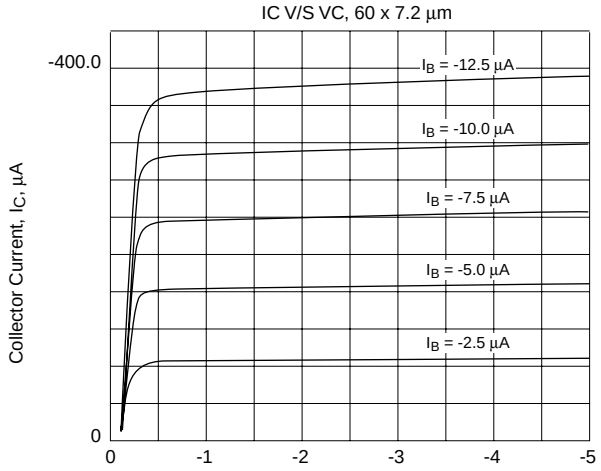
Starting Material	P <100>	N+/P+ Width/Space	1.4 / 1.6µm
Starting Mat. Resistivity	25 - 50 Ω-cm	N+ To P+ Space	5.9µm
Typ. Operating Voltage	5V	Contact To Poly Space	0.8µm
Well Type	N-well	Contact Overlap Of Diffusion	0.7µm
Metal Layers	2	Contact Overlap Of Poly	0.7µm
Poly Layers	2	Metal-1 Overlap Of Contact	0.7µm
Contact Size	0.8x0.8µm	Metal-1 Overlap Of Via	0.7µm
Via Size	0.8x0.8µm	Metal-2 Overlap Of Via	0.7µm
Metal-1 Width/Space	1.4 / 1.0µm	Minimum Pad Opening	65x65µm
Metal-2 Width/Space	1.4 / 1.1µm	Minimum Pad-to-Pad Spacing	5.0µm
Gate Poly Width/Space	0.8 / 1.0µm	Minimum Pad Pitch	80.0µm



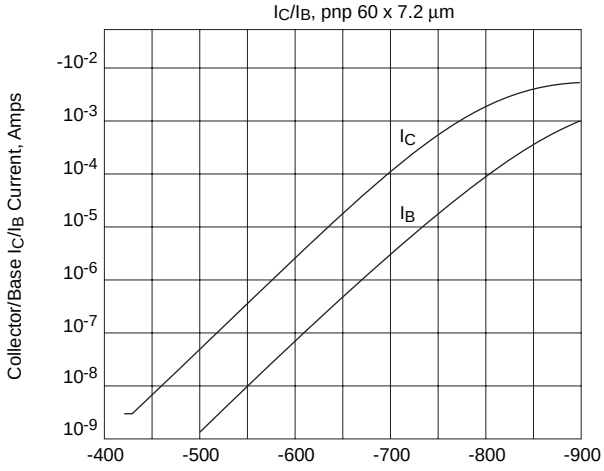
C0809 - n - Channel Transistor Characteristics



C0809 - P - Channel Transistor Characteristics



C0809 Vertical pnp Transistor Characteristics



C0809 Vertical pnp Transistor Characteristics

Process C0810
CMOS 0.8µm
High-Resistance Poly for Analog

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_N	0.6	0.8	1.0	V	100x0.8µm
Body Factor	γ_N		0.74		$V^{1/2}$	100x0.8µm
Conduction Factor	β_N	75	94	115	µA/V²	100x100µm
Effective Channel Length	$Leff_N$		0.8		µm	100x0.8µm
Width Encroachment	ΔW_N		0.3		µm	Per side
Punch Through Voltage	$BVDSS_N$	7	13		V	
Poly Field Threshold	$VTF_{P(N)}$	10	17		V	

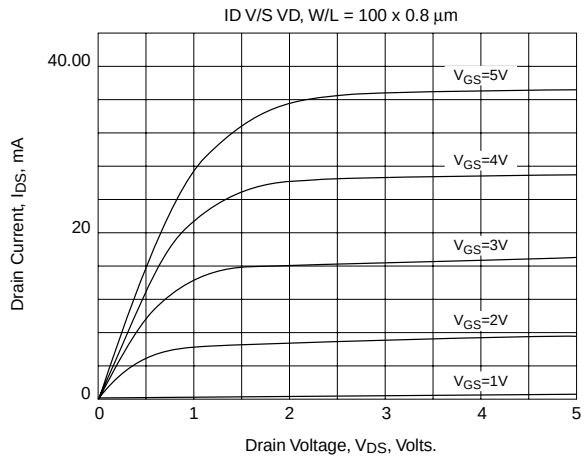
P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_P	–0.7	–0.9	–1.1	V	100x0.8µm
Body Factor	γ_P		0.57		$V^{1/2}$	100x0.8µm
Conduction Factor	β_P	25	31	37	µA/V²	100x100µm
Effective Channel Length	$Leff_P$		0.85		µm	100x0.8µm
Width Encroachment	ΔW_P		0.4		µm	Per side
Punch Through Voltage	$BVDSS_P$	–7	–12		V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–10	–17		V	

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{N\text{-well(f)}}$	0.50	0.65	0.80	KΩ/□	n-well
N+ Sheet Resistance	ρ_{N+}	45	60	75	Ω/□	
N+ Junction Depth	x_{jN+}		0.25		µm	
P+ Sheet Resistance	ρ_{P+}	68	90	112	Ω/□	
P+ Junction Depth	x_{jP+}		0.4		µm	
Gate Oxide Thickness	T_{GOX}		17.5		nm	
Field Oxide Thickness	T_{FIELD}		700		nm	
Bottom Poly Sheet Res.	ρ_{POLY1}	15	23	32	Ω/□	
Gate Poly Sheet Resistance	ρ_{POLY2}	15	23	32	Ω/□	
Metal-1 Sheet Resistance	ρ_{M1}	40	60	80	mΩ/□	
Metal-2 Sheet Resistance	ρ_{M2}	20	30	40	mΩ/□	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.
High Resistance Poly	$\rho_{HI\text{-}POLY}$	1.5	2.0	2.5	KΩ/□	

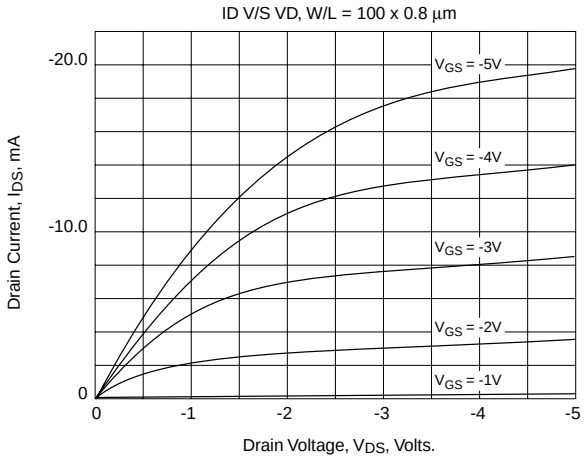
Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}		1.97		fF/µm²	
Metal-1 to Poly1	C_{M1P}		0.046		fF/µm²	
Metal-1 to Silicon	C_{M1S}		0.028		fF/µm²	
Metal-2 to Metal-1	C_{MM}		0.038		fF/µm²	
Poly-1 to Poly-2	C_{PP}	0.69	0.822	1.015	fF/µm²	

Physical Characteristics

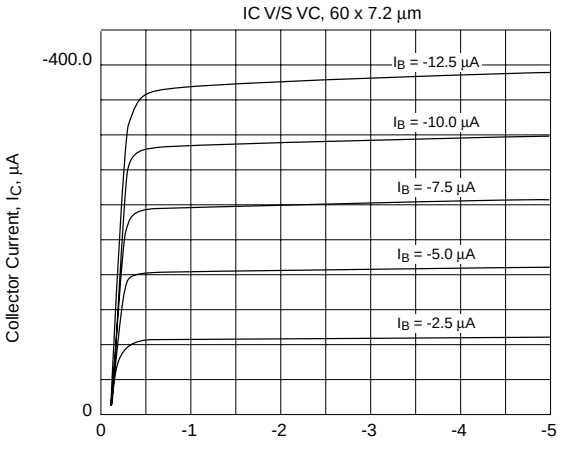
Starting Material	P <100>	N+/P+ Width/Space	1.4 / 1.6µm
Starting Mat. Resistivity	25 - 50 Ω-cm	N+ To P+ Space	5.9µm
Typ. Operating Voltage	5V	Contact To Poly Space	0.8µm
Well Type	N-well	Contact Overlap Of Diffusion	0.7µm
Metal Layers	2	Contact Overlap Of Poly	0.7µm
Poly Layers	2	Metal-1 Overlap Of Contact	0.7µm
Contact Size	0.8x0.8µm	Metal-1 Overlap Of Via	0.7µm
Via Size	0.8x0.8µm	Metal-2 Overlap Of Via	0.7µm
Metal-1 Width/Space	1.4 / 1.0µm	Minimum Pad Opening	65x65µm
Metal-2 Width/Space	1.4 / 1.1µm	Minimum Pad-to-Pad Spacing	5.0µm
Gate Poly Width/Space	0.8 / 1.0µm	Minimum Pad Pitch	80.0µm



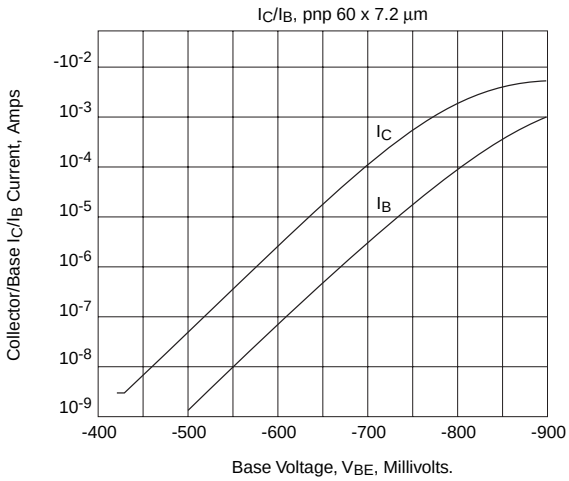
C0810 - n - Channel Transistor Characteristics



C0810 - P - Channel Transistor Characteristics



C0810 Vertical pnp Transistor Characteristics



C0810 Vertical pnp Transistor Characteristics

Process C1004
CMOS 1.0µm
5 Volt Digital

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_N	0.55	0.75	0.95	V	100x1.0µm
Body Factor	γ_N		0.60		$V^{1/2}$	100x1.0µm
Conduction Factor	β_N	74	87	100	µA/V²	100x100µm
Effective Channel Length	$Leff_N$	0.60	0.75	0.90	µm	100x1.0µm
Width Encroachment	ΔW_N		0.8		µm	Per side
Punch Through Voltage	$BVDSS_N$	7			V	
Poly Field Threshold	$VTF_{P(N)}$	10			V	

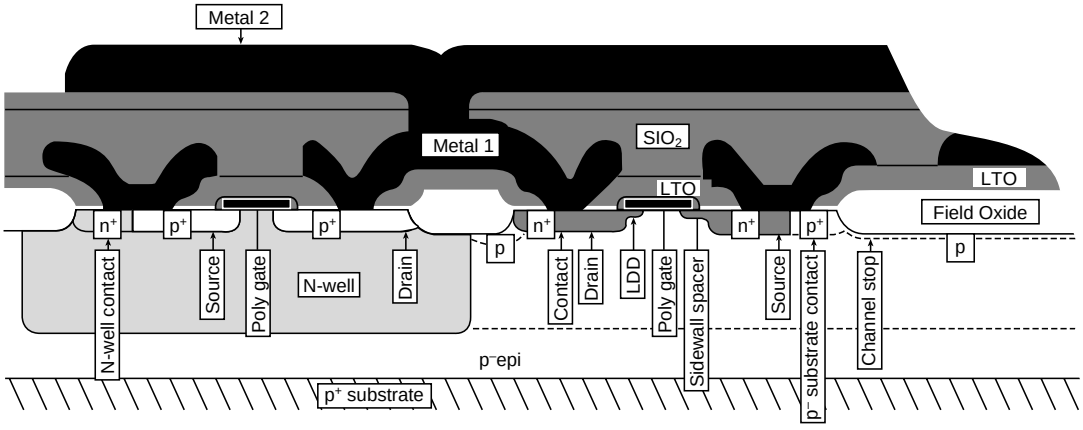
P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_P	–0.85	–1.0	–1.15	V	100x1.0µm
Body Factor	γ_P		0.4		$V^{1/2}$	100x1.0µm
Conduction Factor	β_P	24	28	32	µA/V²	100x100µm
Effective Channel Length	$Leff_P$	0.83	0.98	1.13	µm	100x1.0µm
Width Encroachment	ΔW_P		0.85		µm	Per side
Punch Through Voltage	$BVDSS_P$	–7			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–10			V	

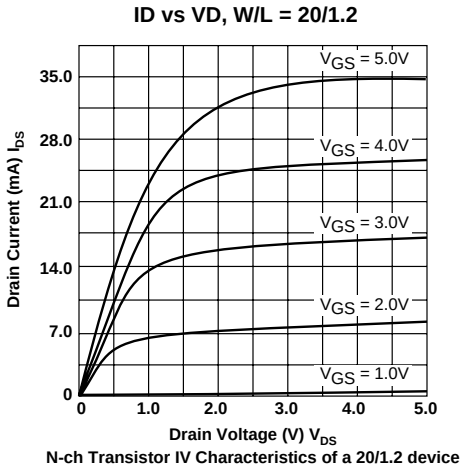
Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{N\text{-well(f)}}$	0.8	1.0	1.22	KΩ/□	n-well
N+ Sheet Resistance	ρ_{N+}	20	35	50	Ω/□	
N+ Junction Depth	x_{jN+}		0.45		µm	
P+ Sheet Resistance	ρ_{P+}	60	80	100	Ω/□	
P+ Junction Depth	x_{jP+}		0.5		µm	
Gate Oxide Thickness	T_{GOX}		20		nm	
Field Oxide Thickness	T_{FIELD}		700		nm	
Poly Sheet Resistance	ρ_{POLY}	15	22	30	Ω/□	
Metal-1 Sheet Resistance	ρ_{M1}		50		mΩ/□	
Metal-2 Sheet Resistance	ρ_{M2}		30		mΩ/□	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{ox}	1.52	1.64	1.82	fF/µm²	
Metal-1 to Poly1	C_{M1P}		0.046		fF/µm²	
Metal-1 to SIlicon	C_{MIS}		0.028		fF/µm²	
Metal-2 to Metal-1	C_{MM}		0.038		fF/µm²	

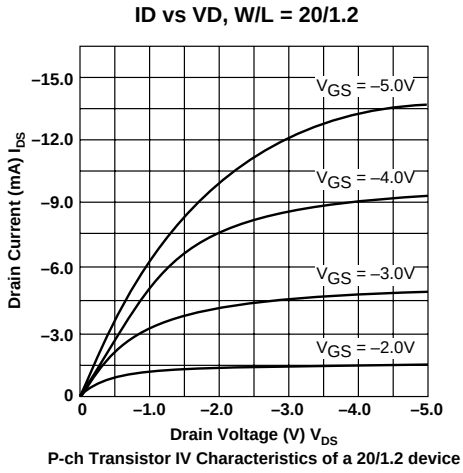
Physical Characteristics

Starting Material	P <100>	N+/P+ Width/Space	2.0 / 1.2µm
Starting Mat. Resistivity	7-8.5 Ω-cm	N+ To P+ Space	7.0µm
Typ. Operating Voltage	5V	Contact To Poly Space	0.8µm
Well Type	N-well	Contact Overlap Of Diffusion	0.7µm
Metal Layers	2	Contact Overlap Of Poly	0.7µm
Poly Layers	1	Metal-1 Overlap Of Contact	0.7µm
Contact Size	1.2x1.2µm	Metal-1 Overlap Of Via	0.7µm
Via Size	1.2x1.2µm	Metal-2 Overlap Of Via	0.7µm
Metal-1 Width/Space	1.4 / 1.2µm	Minimum Pad Opening	65x65µm
Metal-2 Width/Space	2.0 / 1.4µm	Minimum Pad-to-Pad Spacing	5.0µm
Gate Poly Width/Space	1.0 / 1.4µm	Minimum Pad Pitch	80.0µm





N-ch Transistor IV Characteristics of a 20/1.2 device



P-ch Transistor IV Characteristics of a 20/1.2 device

Process C1012
CMOS 1.0µm
5 Volt Digital

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_N	0.725	0.875	1.025	V	100x1.0µm
Body Factor	γ_N		0.76		$V^{1/2}$	100x1.0µm
Conduction Factor	β_N	83	93	103	$\mu A/V^2$	100x100µm
Effective Channel Length	$Leff_N$		0.73		µm	100x1.0µm
Width Encroachment	ΔW_N		0.81		µm	Per side
Punch Through Voltage	$BVDSS_N$	10			V	
Poly Field Threshold	$VTF_{P(N)}$	10			V	

P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_P	–0.86	–1.01	–1.16	V	100x1.0µm
Body Factor	γ_P		0.64		$V^{1/2}$	100x1.0µm
Conduction Factor	β_P	29.5	30.5	33.5	$\mu A/V^2$	100x100µm
Effective Channel Length	$Leff_P$		0.98		µm	100x1.0µm
Width Encroachment	ΔW_P		0.75		µm	Per side
Punch Through Voltage	$BVDSS_P$	–10			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–10			V	

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{N\text{-well(f)}}$	0.565	0.644	0.720	KΩ/□	n-well
N+ Sheet Resistance	ρ_{N+}	20	35	50	Ω/□	
N+ Junction Depth	x_{jN+}		0.45		µm	
P+ Sheet Resistance	ρ_{P+}	60	80	100	Ω/□	
P+ Junction Depth	x_{jP+}		0.5		µm	
Gate Oxide Thickness	T_{GOX}	15.5	17.5	19.5	nm	
Field Oxide Thickness	T_{FIELD}		700		nm	
Poly Sheet Resistance	ρ_{POLY}	15	22	30	Ω/□	
Metal-1 Sheet Resistance	ρ_{M1}	25	45	655	mΩ/□	
Metal-2 Sheet Resistance	ρ_{M2}	15	25	35	mΩ/□	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}		1.97		$fF/\mu m^2$	
Metal-1 to Poly1	C_{M1P}		0.046		$fF/\mu m^2$	
Metal-1 to Silicon	C_{M1S}		0.028		$fF/\mu m^2$	
Metal-2 to Metal-1	C_{MM}		0.038		$fF/\mu m^2$	

Physical Characteristics

Starting Material	P <100>	N+/P+ Width/Space	2.0 / 1.2µm
Starting Mat. Resistivity	25 - 50 Ω-cm	N+ To P+ Space	5.0µm
Typ. Operating Voltage	5V	Contact To Poly Space	1.0µm
Well Type	N-well	Contact Overlap Of Diffusion	1.0µm
Metal Layers	2	Contact Overlap Of Poly	0.8µm
Poly Layers	1	Metal-1 Overlap Of Contact	0.8µm
Contact Size	1.2 x 1.2µm	Metal-1 Overlap Of Via	0.8µm
Via Size	1.2 x 1.2µm	Metal-2 Overlap Of Via	0.8µm
Metal-1 Width/Space	1.4 / 2.4µm	Minimum Pad Opening	65 x 65µm
Metal-2 Width/Space	2.0 / 1.4µm	Minimum Pad-to-Pad Spacing	5.0µm
Gate Poly Width/Space	1.0 / 1.4µm	Minimum Pad Pitch	80.0µm

Process C1015
CMOS 1.0µm
Analog Mixed Mode

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_N	0.65	0.85	1.05	V	25 x 1.0µm
Body Factor	γ_N	0.72	0.82	0.92	$V^{1/2}$	25 x 1.0µm
Conduction Factor	β_N	40.0	43.5	47.0	$\mu A/V^2$	25 x 25µm
Effective Channel Length	$Leff_N$	0.70	0.90	1.10	µm	25 x 1.0µm
Width Encroachment	ΔW_N		0.25		µm	Per side
Punch Through Voltage	$BVDSS_N$	8			V	
Poly Field Threshold	$VTF_{P(N)}$	8			V	

P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_P	–1.3	–1.1	–0.9	V	25 x 1.0µm
Body Factor	γ_P	0.46	0.56	0.66	$V^{1/2}$	25 x 1.0µm
Conduction Factor	β_P	12.5	14.0	15.5	$\mu A/V^2$	25 x 25µm
Effective Channel Length	$Leff_P$	0.72	0.97	1.22	µm	25 x 1.0µm
Width Encroachment	ΔW_P		0.3		µm	Per side
Punch Through Voltage	$BVDSS_P$	–8			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–8			V	

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{N\text{-well(f)}}$	0.65	0.80	1.10	KΩ/□	n-well
N+ Sheet Resistance	ρ_{N+}	27	37	47	Ω/□	
N+ Junction Depth	x_{jN+}		0.25		µm	
P+ Sheet Resistance	ρ_{P+}	65	85	110	Ω/□	
P+ Junction Depth	x_{jP+}		0.3		µm	
Gate Oxide Thickness	T_{GOX}	18.7	20.0	21.3	nm	
Field Oxide Thickness	T_{FIELD}		580		nm	
Gate Poly Sheet Res.	ρ_{POLY1}	25	32	39	Ω/□	
Top Poly Sheet Resistance	ρ_{POLY2}	18	23	28	Ω/□	
Metal-1 Sheet Resistance	ρ_{M1}		45		mΩ/□	
Metal-2 Sheet Resistance	ρ_{M2}		25		mΩ/□	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}		1.73		$fF/\mu m^2$	
Metal-1 to Poly1	C_{M1P}		0.046		$fF/\mu m^2$	
Metal-1 to Silicon	C_{M1S}		0.028		$fF/\mu m^2$	
Metal-2 to Metal-1	C_{MM}		0.035		$fF/\mu m^2$	
Poly-1 to Poly-2	C_{P1P2}	0.42	0.5	0.57	$fF/\mu m^2$	

Physical Characteristics

Starting Material	P <100>	N+/P+ Width/Space	1.6 / 1.6µm
Starting Mat. Resistivity	15 - 25 Ω-cm	N+ To P+ Space	7.0µm
Typ. Operating Voltage	5V	Contact To Poly Space	1.0µm
Well Type	N-well	Contact Overlap Of Diffusion	1.0µm
Metal Layers	2	Contact Overlap Of Poly	0.8µm
Poly Layers	2	Metal-1 Overlap Of Contact	0.8µm
Contact Size	1.2x1.2µm	Metal-1 Overlap Of Via	0.8µm
Via Size	1.2x1.2µm	Metal-2 Overlap Of Via	0.8µm
Metal-1 Width/Space	1.4 / 1.2µm	Minimum Pad Opening	65x65µm
Metal-2 Width/Space	2.5 / 1.5µm	Minimum Pad-to-Pad Spacing	5.0µm
Gate Poly Width/Space	1.5 / 2.0µm	Minimum Pad Pitch	80.0µm

Special Feature of C1015 Process: CMOS 1.0 µm analog technology with 2 levels of metal and Poly-to-Poly capacitors for analog applications.

Process C1026
BiCMOS 1.0μm
Schottky Diode and Low TC P-Poly Resistor

Electrical Characteristics

T=25°C Unless otherwise noted

	Symbol	Minimum	Typical	Maximum	Unit	Comments
N-Channel High Voltage Transistor						
Threshold Voltage	HVT_N	0.50	0.70	0.90	V	
Punch Through Voltage	$HVBVDSS_N$	25			V	
ON Resistance	$HVPR_{0N}$	200	240	350	Ω	V_{DS} = 0.1V V_{GS} = 5.0V 100x3.0μm
Operating Voltage				V_{GS} = 5V V_{DS} = 20V	V	
N-Channel Low Voltage Transistor						
Threshold Voltage	VT_N	0.65	0.85	1.05	V	100x1.0μm
Body Factor	γ_N	0.75	0.82	0.95	$V^{1/2}$	100x1.0μm
Conduction Factor	β_N	79.0	87.0	95.0	μA/V²	100x100μm
Effective Channel Length	$Leff_N$	0.70	0.90	1.10	μm	100x1.0μm
Width Encroachment	ΔW_N		0.60		μm	Per side
Punch Through Voltage	$BVDSS_N$	8	13		V	
Poly Field Threshold Voltage	$VTFP_N$	14	18		V	

	Symbol	Minimum	Typical	Maximum	Unit	Comments
P-Channel High Voltage Transistor						
Threshold Voltage	HVT_P	–0.8	–1.0	–1.2	V	
Punch Through Voltage	$HVBVDSS_P$	–25			V	
ON Resistance	$HVPR_{0N}$	400	450	600	Ω	V_{DS} = 0.1V V_{GS} = 5.0V 100x3.5μm
Operating Voltage				V_{GS} = –5V V_{DS} = –20V	V	
P-Channel Low Voltage Transistor						
Threshold Voltage	VT_P	–1.25	–1.0	–0.85	V	100x1.0μm
Body Factor	γ_P	0.40	0.50	0.60	$V^{1/2}$	100x1.0μm
Conduction Factor	β_P	24.0	28.0	32.0	μA/V²	100x100μm
Effective Channel Length	$Leff_P$	0.72	0.97	1.12	μm	100x1.0μm
Width Encroachment	ΔW_P		0.60		μm	Per side
Punch Through Voltage	$BVDSS_P$	–8	–12		V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–14	–18		V	

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}		1.727		fF/μm²	
Metal-1 to Poly1	C_{M1P}		0.046		fF/μm²	
Metal-2 to Metal-1	C_{MM}		0.038		fF/μm²	

Electrical Characteristics

Vertical NPN Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Beta	h_{FE}	50	100	150		4.5x4.5mm
Early Voltage	V_{AN}	30	34			
Cut-Off Frequency	f_τ		6.2		GHz	

Lateral PNP	Symbol	Minimum	Typical	Maximum	Unit	Comments
Beta	h_{FE}	10	40	100		

Schottky Diode	Symbol	Minimum	Typical	Maximum	Unit	Comments
Reverse Bias Breakdown Voltage		–18	–20		V	10x10µm
Forware Bias Voltage		0.10	0.15	0.20	V	
ON Resistance			175		Ω	10x10µm

Low TCR P-Poly Resistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Resistivity		180	230	290	Ω/□	
TCR		–100	0	+50	ppm/°C	

Physical Characteristics

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Starting Material p<100>		25		50	Ω-cm	
Well (field) Sheet Resistance	$\rho_{N\text{-}well(f)}$	0.65	0.80	1.10	KΩ/□	n-well
N+ Sheet Resistance	ρ_{N+}	22.0	37.0	50.0	Ω/□	
N+ Junction Depth	x_{jN+}		0.45		µm	
P+ Sheet Resistance	ρ_{P+}	40.0	57.0	80.0	Ω/□	
P+ Junction Depth	x_{jP+}		0.50		µm	
High-Voltage Gate Oxide Th	HT_{GOX}		20		nm	
Gate Oxide Thickness	T_{GOX}		20		nm	
Interpoly Oxide Thickness	$I\rho_{OX}$		47			
Gate Poly Sheet Resistance	ρ_{POLY1}	23.0	38.0	53.0	Ω/□	
Metal-1 Sheet Resistance	ρ_{M1}	35.0	45.0	65.0	mΩ/□	
Metal-2 Sheet Resistance	ρ_{M2}	19.0	25.0	35.0	mΩ/□	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Layout Rules

Min Channel Width	2.0µm	Contact to Poly Space	1.0µm
Min spacing, active region, 5V	1.2µm	Contact Overlap of Diffusion	1.0µm
Min spacing, active region, 12V	2.0µm		
Poly1 (Gate) Width/Space	1.0/1.4µm	Contact Overlap of Poly	0.8µm
Poly2 Width/Space	1.6/2.0µm	Metal-1 Overlap of Contact	0.8µm
Contact Width/Space	1.2x1.2µm	Metal-1 Overlap of Via	0.8µm
Metal-1 Width/Space	1.4/1.2µm	Minimum Pad Opening	65x65µm
Metal-2 Width/Space	1.8/1.4µm	Minimum Pad to Pad Spacing	5.0µm
Via Width/Space	1.2/1.8µm	Minimum Pad Pitch	80µm

Process C1027
BiCMOS 1.0µm
Low TC P-Poly Resistor

Electrical Characteristics

T=25°C Unless otherwise noted

	Symbol	Minimum	Typical	Maximum	Unit	Comments
N-Channel High Voltage Transistor						
Threshold Voltage	HVT_N	0.50	0.70	0.90	V	
Punch Through Voltage	$HVBVDSS_N$	25			V	
ON Resistance	$HVPR_{0N}$	200	240	350	Ω	100x2.0µm
Operating Voltage				V_{GS} = 5V V_{DS} = 20V	V	
N-Channel Low Voltage Transistor						
Threshold Voltage	VT_N	0.65	0.85	1.05	V	100x1.0µm
Body Factor	γ_N	0.75	0.85	0.95	$V^{1/2}$	100x1.0µm
Conduction Factor	β_N	79.0	87.0	95.0	$\mu A/V^2$	100x100µm
Effective Channel Length	$Leff_N$	0.70	0.90	1.10	µm	100x1.0µm
Width Encroachment	ΔW_N		0.60		µm	Per side
Punch Through Voltage	$BVDSS_N$	8	13		V	
Poly Field Threshold Voltage	$VTFP_N$	14	18		V	

	Symbol	Minimum	Typical	Maximum	Unit	Comments
P-Channel Low Voltage Transistor						
Threshold Voltage	VT_P	–1.25	–1.05	–0.85	V	100x1.0µm
Body Factor	γ_P	0.4	0.5	0.6	$V^{1/2}$	100x1.0µm
Conduction Factor	β_P	24.0	28.0	32.0	$\mu A/V^2$	100x100µm
Effective Channel Length	$Leff_P$	0.72	0.97	1.12	µm	100x1.0µm
Width Encroachment	ΔW_P		0.60		µm	Per side
Punch Through Voltage	$BVDSS_P$	–8	–12		V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–14	–18		V	

Capacitance	**Symbol**	**Minimum**	**Typical**	**Maximum**	**Unit**	**Comments**
Gate Oxide	C_{OX}		1.727		$fF/\mu m^2$	
Metal-1 to Poly1	C_{M1P}		0.046		$fF/\mu m^2$	
Metal-2 to Metal-1	C_{MM}		0.038		$fF/\mu m^2$	

Electrical Characteristics

Vertical NPN Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Beta	h_{FE}	50	100	150		4.5x4.5mm
Early Voltage	V_{AN}	30	34			
Cut-Off Frequency	f_τ		6.2		GHz	

Lateral PNP	Symbol	Minimum	Typical	Maximum	Unit	Comments
Beta	h_{FE}	10	40	100		
Early Voltage	V_{AP}		TBD		V	

Low TCR P-Poly Resistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Resistivity		180	230	290	Ω/☐	
TCR		–100	0	+50	ppm/°C	

Physical Characteristics

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Starting Material p<100>		25		50	Ω-cm	
Well (field) Sheet Resistance	$\rho_{N\text{-}well(f)}$	0.65	0.80	1.10	KΩ/☐	n-well
N+ Sheet Resistance	ρ_{N+}	22.0	37.0	50.0	Ω/☐	
N+ Junction Depth	x_{jN+}		0.45		µm	
P+ Sheet Resistance	ρ_{P+}	40.0	57.0	80.0	Ω/☐	
P+ Junction Depth	x_{jP+}		0.50		µm	
High-Voltage Gate Oxide Th	HT_{GOX}		20		nm	
Gate Oxide Thickness	T_{GOX}		20		nm	
Interpoly Oxide Thickness	$I\rho_{OX}$		47		nm	
Gate Poly Sheet Resistance	ρ_{POLY1}	23.0	38.0	53.0	Ω/☐	
Metal-1 Sheet Resistance	ρ_{M1}	35.0	45.0	65.0	mΩ/☐	
Metal-2 Sheet Resistance	ρ_{M2}	19.0	25.0	35.0	mΩ/☐	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Layout Rules

Min Channel Width	2.0µm	Contact to Poly Space	1.0µm
Min spacing, active region, 5V	1.2µm	Contact Overlap of Diffusion	1.0µm
Min spacing, active region, 12V	2.0µm		
Poly1 (Gate) Width/Space	1.0/1.4µm	Contact Overlap of Poly	0.8µm
Poly2 Width/Space	1.6/2.0µm	Metal-1 Overlap of Contact	0.8µm
Contact Width/Space	1.2x1.2µm	Metal-1 Overlap of Via	0.8µm
Metal-1 Width/Space	1.4/1.2µm	Minimum Pad Opening	65x65µm
Metal-2 Width/Space	1.8/1.4µm	Minimum Pad to Pad Spacing	5.0µm
Via Width/Space	1.2/1.8µm	Minimum Pad Pitch	80µm

Process C1028
BiCMOS 1.0μm
Low TC P-Poly Resistor

Electrical Characteristics

T=25°C Unless otherwise noted

	Symbol	Minimum	Typical	Maximum	Unit	Comments
N-Channel High Voltage Transistor						
Threshold Voltage	HVT_N	0.50	0.70	0.90	V	
Punch Through Voltage	$HVBVDSS_N$	25			V	
ON Resistance	$HVPR_{0N}$	200	240	350	Ω	100x2.0μm
Operating Voltage				V_{GS} = 5V V_{DS} = 20V	V	
N-Channel Low Voltage Transistor						
Threshold Voltage	VT_N	0.65	0.85	1.05	V	100x1.0μm
Body Factor	γ_N	0.75	0.85	0.95	$V^{1/2}$	100x1.0μm
Conduction Factor	β_N	79.0	87.0	95.0	$\mu A/V^2$	100x100μm
Effective Channel Length	$Leff_N$	0.70	0.90	1.10	μm	100x1.0μm
Width Encroachment	ΔW_N		0.60		μm	Per side
Punch Through Voltage	$BVDSS_N$	8	13		V	
Poly Field Threshold Voltage	$VTFP_N$	14	18		V	

	Symbol	Minimum	Typical	Maximum	Unit	Comments
P-Channel High Voltage Transistor						
Threshold Voltage	HVT_P	–0.8	–1.0	–1.2	V	
Punch Through Voltage	$HVBVDSS_P$	–25			V	
ON Resistance	$HVPR_{0N}$	400	450	600	Ω	100x3.0μm
Operating Voltage		–15		V_{GS} = –5V V_{DS} = –20V	V	
P-Channel Low Voltage Transistor						
Threshold Voltage	VT_P	–1.25	–1.05	–0.85	V	100x1.0μm
Body Factor	γ_P	0.40	0.50	0.60	$V^{1/2}$	100x1.0μm
Conduction Factor	β_P	24.0	28.0	32.0	$\mu A/V^2$	100x100μm
Effective Channel Length	$Leff_P$	0.72	0.97	1.12	μm	100x1.0μm
Width Encroachment	ΔW_P		0.60		μm	Per side
Punch Through Voltage	$BVDSS_P$	–8	–12		V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–14	–18		V	

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}		1.727		$fF/\mu m^2$	
Metal-1 to Poly1	C_{M1P}		0.046		$fF/\mu m^2$	
Metal-2 to Metal-1	C_{MM}		0.038		$fF/\mu m^2$	

Electrical Characteristics

Vertical NPN Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Beta	h_{FE}	50	100	150		4.5x4.5mm
Early Voltage	V_{AN}	30	34			
Cut-Off Frequency	f_τ		6.2		GHz	

Lateral PNP	Symbol	Minimum	Typical	Maximum	Unit	Comments
Beta	h_{FE}	10	40	100		
Early Voltage	V_{AP}		TBD		V	

Low TCR P-Poly Resistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Resistivity		180	230	290	Ω/☐	
TCR		–100	0	+50	ppm/°C	

Physical Characteristics

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Starting Material p<100>		25		50	Ω-cm	
Well (field) Sheet Resistance	$\rho_{N\text{-}well(f)}$	0.65	0.80	1.10	KΩ/☐	n-well
N+ Sheet Resistance	ρ_{N+}	22.0	37.0	50.0	Ω/☐	
N+ Junction Depth	x_{jN+}		0.45		µm	
P+ Sheet Resistance	ρ_{P+}	40.0	57.0	80.0	Ω/☐	
P+ Junction Depth	x_{jP+}		0.50		µm	
High-Voltage Gate Oxide Th	HT_{GOX}		20		nm	
Gate Oxide Thickness	T_{GOX}		20		nm	
Interpoly Oxide Thickness	$I\rho_{OX}$		47			
Gate Poly Sheet Resistance	ρ_{POLY1}	23.0	38.0	53.0	Ω/☐	
Metal-1 Sheet Resistance	ρ_{M1}	35.0	45.0	65.0	mΩ/☐	
Metal-2 Sheet Resistance	ρ_{M2}	19.0	25.0	35.0	mΩ/☐	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Layout Rules

Min Channel Width	2.0µm	Contact to Poly Space	1.0µm
Min spacing, active region, 5V	1.2µm	Contact Overlap of Diffusion	1.0µm
Min spacing, active region, 12V	2.0µm		
Poly1 (Gate) Width/Space	1.0/1.4µm	Contact Overlap of Poly	0.8µm
Poly2 Width/Space	1.6/2.0µm	Metal-1 Overlap of Contact	0.8µm
Contact Width/Space	1.2x1.2µm	Metal-1 Overlap of Via	0.8µm
Metal-1 Width/Space	1.4/1.2µm	Minimum Pad Opening	65x65µm
Metal-2 Width/Space	1.8/1.4µm	Minimum Pad to Pad Spacing	5.0µm
Via Width/Space	1.2/1.8µm	Minimum Pad Pitch	80µm

Process C1029
BiCMOS 1.0µm
Schottky Diode and High-Resistance P-Poly Resistor

Electrical Characteristics

T=25°C Unless otherwise noted

	Symbol	Minimum	Typical	Maximum	Unit	Comments
N-Channel High Voltage Transistor						
Threshold Voltage	HVT_N	0.50	0.70	0.90	V	
Punch Through Voltage	$HVBVDSS_N$	25			V	
ON Resistance	$HVPR_{0N}$	200	240	350	Ω	100x2.0µm
Operating Voltage				V_{GS} = 5V V_{DS} = 20V	V	
N-Channel Low Voltage Transistor						
Threshold Voltage	VT_N	0.65	0.85	1.05	V	100x1.0µm
Body Factor	γ_N	0.75	0.85	0.95	$V^{1/2}$	100x1.0µm
Conduction Factor	β_N	79.0	87.0	95.0	$\mu A/V^2$	100x100µm
Effective Channel Length	$Leff_N$	0.70	0.90	1.10	µm	100x1.0µm
Width Encroachment	ΔW_N		0.60		µm	Per side
Punch Through Voltage	$BVDSS_N$	8	13		V	
Poly Field Threshold Voltage	$VTFP_N$	14	18		V	

	Symbol	Minimum	Typical	Maximum	Unit	Comments
P-Channel High Voltage Transistor						
Threshold Voltage	HVT_P	–0.8	–1.0	–1.2	V	
Punch Through Voltage	$HVBVDSS_P$	–25			V	
ON Resistance	$HVPR_{0N}$	400	450	600	Ω	100x3.0µm
Operating Voltage				V_{GS} = –5V V_{DS} = –20V	V	
P-Channel Low Voltage Transistor						
Threshold Voltage	VT_P	–1.25	–1.05	–0.85	V	100x1.0µm
Body Factor	γ_P	0.40	0.50	0.60	$V^{1/2}$	100x1.0µm
Conduction Factor	β_P	24.0	28.0	32.0	$\mu A/V^2$	100x100µm
Effective Channel Length	$Leff_P$	0.72	0.97	1.12	µm	100x1.0µm
Width Encroachment	ΔW_P		0.60		µm	Per side
Punch Through Voltage	$BVDSS_P$	–8	–12		V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–14	–18		V	

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}		1.727		$fF/\mu m^2$	
Metal-1 to Poly1	C_{M1P}		0.046		$fF/\mu m^2$	
Metal-2 to Metal-1	C_{MM}		0.038		$fF/\mu m^2$	

Electrical Characteristics

Vertical NPN Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Beta	h_{FE}	50	100	150		4.5x4.5mm
Early Voltage	V_{AN}	30	34			
Cut-Off Frequency	f_τ		6.2		GHz	

Lateral PNP	Symbol	Minimum	Typical	Maximum	Unit	Comments
Beta	h_{FE}	10	40	100		
Early Voltage	V_{AP}		TBD		V	

Schottky Diode	Symbol	Minimum	Typical	Maximum	Unit	Comments
Reverse Bias Breakdown V			–20		V	
Forward Bias Voltage		0.10	0.15	0.2	V	
ON Resistance			190		Ω	10x10µm

Low TCR P-Poly Resistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
High-Resistance P-Poly Resistor		1500	2000	2500	Ω/□	

Physical Characteristics

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Starting Material p<100>		25		50	Ω-cm	
Well (field) Sheet Resistance	$\rho_{N\text{-}well(f)}$	0.65	0.80	1.10	KΩ/□	n-well
N+ Sheet Resistance	ρ_{N+}	22.0	37.0	50.0	Ω/□	
N+ Junction Depth	x_{jN+}		0.45		µm	
P+ Sheet Resistance	ρ_{P+}	40.0	57.0	80.0	Ω/□	
P+ Junction Depth	x_{jP+}		0.50		µm	
High-Voltage Gate Oxide Th	HT_{GOX}		20		nm	
Gate Oxide Thickness	T_{GOX}		20		nm	
Interpoly Oxide Thickness	$I\rho_{OX}$		45			
Gate Poly Sheet Resistance	ρ_{POLY1}	23.0	38.0	53.0	Ω/□	
Metal-1 Sheet Resistance	ρ_{M1}	35.0	45.0	65.0	mΩ/□	
Metal-2 Sheet Resistance	ρ_{M2}	19.0	25.0	35.0	mΩ/□	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Layout Rules

Min Channel Width	2.0µm	Contact to Poly Space	1.0µm
Min spacing, active region, 5V	1.2µm	Contact Overlap of Diffusion	1.0µm
Min spacing, active region, 12V	2.0µm		
Poly1 (Gate) Width/Space	1.0/1.4µm	Contact Overlap of Poly	0.8µm
Poly2 Width/Space	1.6/2.0µm	Metal-1 Overlap of Contact	0.8µm
Contact Width/Space	1.2x1.2µm	Metal-1 Overlap of Via	0.8µm
Metal-1 Width/Space	1.4/1.2µm	Minimum Pad Opening	65x65µm
Metal-2 Width/Space	1.8/1.4µm	Minimum Pad to Pad Spacing	5.0µm
Via Width/Space	1.2/1.8µm	Minimum Pad Pitch	80µm

Process C1201
CMOS 1.2µm
Digital Double-Metal

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_N	0.55	0.75	0.95	V	100x1.2µm
Body Factor	γ_N		0.34		$V^{1/2}$	100x1.2µm
Conduction Factor	β_N	64	75	86	$\mu A/V^2$	100x100µm
Effective Channel Length	$Leff_N$	0.8	1.0	1.2	µm	100x1.2µm
Width Encroachment	ΔW_N		0.6		µm	Per side
Punch Through Voltage	$BVDSS_N$	9			V	
Poly Field Threshold	$VTF_{P(N)}$	10			V	

P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_P	–0.7	–0.9	–1.1	V	100x1.2µm
Body Factor	γ_P		0.38		$V^{1/2}$	100x1.2µm
Conduction Factor	β_P	21	25	29	$\mu A/V^2$	100x100µm
Effective Channel Length	$Leff_P$	0.9	1.1	1.3	µm	100x1.2µm
Width Encroachment	ΔW_P		0.8		µm	Per side
Punch Through Voltage	$BVDSS_P$	–9			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–10			V	

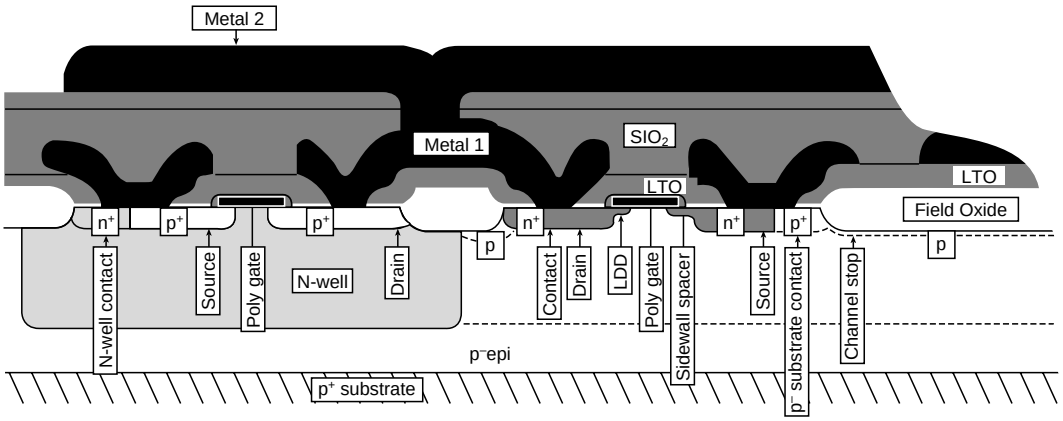
Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{N\text{-well(f)}}$	0.6	1.0	1.3	KΩ/□	n-well
N+ Sheet Resistance	ρ_{N+}	20	35	50	Ω/□	
N+ Junction Depth	x_{jN+}		0.35		µm	
P+ Sheet Resistance	ρ_{P+}	50	75	100	Ω/□	
P+ Junction Depth	x_{jP+}		0.35		µm	
Gate Oxide Thickness	T_{GOX}		24		nm	
Field Oxide Thickness	T_{FIELD}		800		nm	
Gate Poly Sheet Res.	ρ_{POLY1}	15	22	30	Ω/□	
Metal-1 Sheet Resistance	ρ_{M1}		50		mΩ/□	
Metal-2 Sheet Resistance	ρ_{M2}		30		mΩ/□	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}	1.28	1.38	1.58	$fF/\mu m^2$	
Metal-1 to Poly1	C_{M1P}		0.057		$fF/\mu m^2$	
Metal-1 to Silicon	C_{M1S}		0.028		$fF/\mu m^2$	
Metal-2 to Metal-1	C_{MM}		0.035		$fF/\mu m^2$	

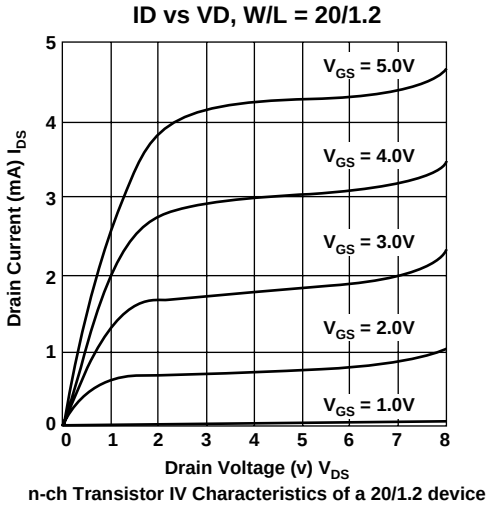
Physical Characteristics

Starting Material	EPI P <100>	N+/P+ Width/Space	2.0 / 1.2µm
Starting Mat. Resistivity	7 - 8.5 Ω-cm	N+ To P+ Space	9.0µm
Typ. Operating Voltage	5V	Contact To Poly Space	1.5µm
Well Type	N-well	Contact Overlap Of Diffusion	1.0µm
Metal Layers	2	Contact Overlap Of Poly	1.0µm
Poly Layers	1	Metal-1 Overlap Of Contact	1.0µm
Contact Size	1.5x1.5µm	Metal-1 Overlap Of Via	1.0µm
Via Size	1.5x1.5µm	Metal-2 Overlap Of Via	1.0µm
Metal-1 Width/Space	2.5 / 1.5µm	Minimum Pad Opening	65x65µm
Metal-2 Width/Space	2.5 / 1.5µm	Minimum Pad-to-Pad Spacing	5.0µm
Gate Poly Width/Space	1.5 / 2.0µm	Minimum Pad Pitch	80.0µm

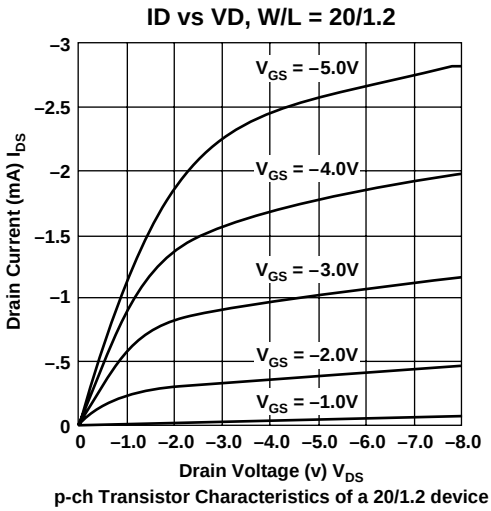
Special Feature of C1201 Process: CMOS 1.2 µm digital technology with 1 poly and 2 levels of metal.



Cross-sectional view of the MxCMOS 1.2 process



n-ch Transistor IV Characteristics of a 20/1.2 device



p-ch Transistor Characteristics of a 20/1.2 device

Process C1202
CMOS 1.2µm
Analog Mixed Mode

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_N	0.55	0.75	0.95	V	100x1.2µm
Body Factor	γ_N		0.34		$V^{1/2}$	100x1.2µm
Conduction Factor	β_N	64	75	86	$\mu A/V^2$	100x100µm
Effective Channel Length	$Leff_N$	0.8	1.0	1.2	µm	100x1.2µm
Width Encroachment	ΔW_N		0.6		µm	Per side
Punch Through Voltage	$BVDSS_N$	9			V	
Poly Field Threshold	$VTF_{P(N)}$	10			V	

P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_P	–0.7	–0.9	–1.1	V	100x1.2µm
Body Factor	γ_P		0.38		$V^{1/2}$	100x1.2µm
Conduction Factor	β_P	21	25	29	$\mu A/V^2$	100x100µm
Effective Channel Length	$Leff_P$	0.9	1.1	1.3	µm	100x1.2µm
Width Encroachment	ΔW_P		0.8		µm	Per side
Punch Through Voltage	$BVDSS_P$	–9			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–10			V	

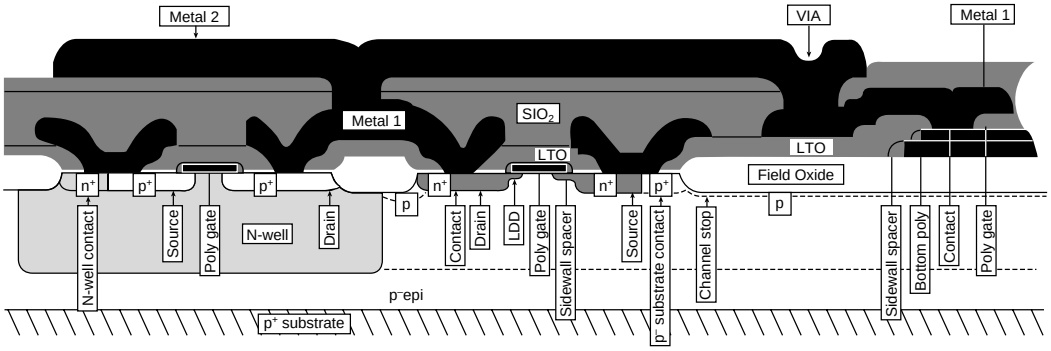
Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{N\text{-well(f)}}$	0.6	1.0	1.3	KΩ/□	n-well
N+ Sheet Resistance	ρ_{N+}	20	35	50	Ω/□	
N+ Junction Depth	x_{jN+}		0.35		µm	
P+ Sheet Resistance	ρ_{P+}	50	75	100	Ω/□	
P+ Junction Depth	x_{jP+}		0.35		µm	
Gate Oxide Thickness	T_{GOX}		24		nm	
Field Oxide Thickness	T_{FIELD}		800		nm	
Gate Poly Sheet Res.	ρ_{POLY2}	15	22	30	Ω/□	
Bottom Poly Sheet Res.	ρ_{POLY1}		35		Ω/□	
Metal-1 Sheet Resistance	ρ_{M1}		50		mΩ/□	
Metal-2 Sheet Resistance	ρ_{M2}		30		mΩ/□	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}	1.28	1.38	1.58	$fF/\mu m^2$	
Metal-1 to Poly1	C_{M1P}		0.057		$fF/\mu m^2$	
Metal-1 to Silicon	C_{M1S}		0.028		$fF/\mu m^2$	
Metal-2 to Metal-1	C_{MM}		0.035		$fF/\mu m^2$	
Poly-1 to Poly-2	C_{P1P2}	0.68	0.86	1.03	$fF/\mu m^2$	

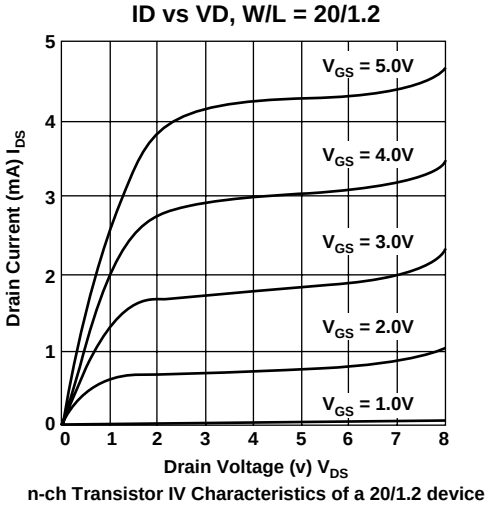
Physical Characteristics

Starting Material	EPI P <100>	N+/P+ Width/Space	2.5 / 2.0µm
Starting Mat. Resistivity	7 - 8.5 Ω-cm	N+ To P+ Space	9.0µm
Typ. Operating Voltage	5V	Contact To Poly Space	1.5µm
Well Type	N-well	Contact Overlap Of Diffusion	1.0µm
Metal Layers	2	Contact Overlap Of Poly	1.0µm
Poly Layers	2	Metal-1 Overlap Of Contact	1.0µm
Contact Size	1.5x1.5µm	Metal-1 Overlap Of Via	1.0µm
Via Size	1.5x1.5µm	Metal-2 Overlap Of Via	1.0µm
Metal-1 Width/Space	2.5 / 1.5µm	Minimum Pad Opening	65x65µm
Metal-2 Width/Space	2.5 / 1.5µm	Minimum Pad-to-Pad Spacing	5.0µm
Gate Poly Width/Space	1.5 / 2.0µm	Minimum Pad Pitch	80.0µm

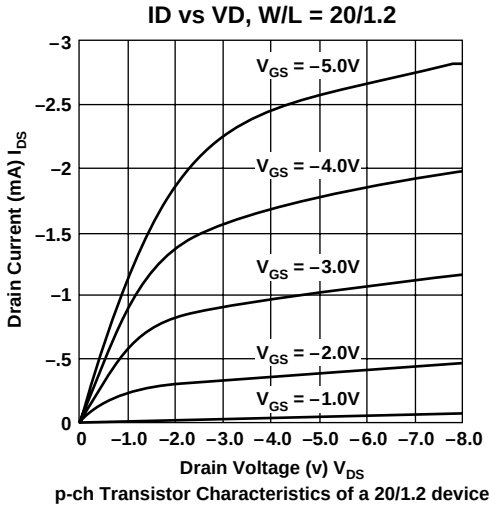
Special Feature of C1202 Process: CMOS 1.2 µm technology with 2 levels of metal and Poly-to-Poly capacitors for analog applications.



Cross-sectional view of the MxCMOS 1.2 process



n-ch Transistor IV Characteristics of a 20/1.2 device



p-ch Transistor Characteristics of a 20/1.2 device

Process C1203
BiCMOS 1.2µm
2.0GHz

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_N	0.55	0.75	0.95	V	100x1.2µm
Body Factor	γ_N		0.34		$V^{1/2}$	100x1.2µm
Conduction Factor	β_N	64	75	86	µA/V²	100x100µm
Effective Channel Length	$Leff_N$	0.8	1.0	1.2	µm	100x1.2µm
Width Encroachment	ΔW_N		0.6		µm	Per side
Punch Through Voltage	$BVDSS_N$	9			V	
Poly Field Threshold	$VTF_{P(N)}$	10			V	

P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_P	–0.7	–0.9	–1.1	V	100x1.2µm
Body Factor	γ_P		0.38		$V^{1/2}$	100x1.2µm
Conduction Factor	β_P	21	25	29	µA/V²	100x100µm
Effective Channel Length	$Leff_P$	0.9	1.1	1.3	µm	100x1.2µm
Width Encroachment	ΔW_P		0.8		µm	Per side
Punch Through Voltage	$BVDSS_P$	–9			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–10			V	

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{N\text{-well(f)}}$	0.6	1.0	1.3	KΩ/□	n-well
N+ Sheet Resistance	ρ_{N+}	20	35	50	Ω/□	
N+ Junction Depth	x_{jN+}		0.35		µm	
P+ Sheet Resistance	ρ_{P+}	50	75	100	Ω/□	
P+ Junction Depth	x_{jP+}		0.35		µm	
Gate Oxide Thickness	T_{GOX}		24		nm	
Field Oxide Thickness	T_{FIELD}		800		nm	
Gate Poly Sheet Res.	ρ_{POLY2}	15	22	30	Ω/□	
Bottom Poly Sheet Res.	ρ_{POLY1}		35		Ω/□	
Metal-1 Sheet Resistance	ρ_{M1}		50		mΩ/□	
Metal-2 Sheet Resistance	ρ_{M2}		30		mΩ/□	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}	1.28	1.38	1.58	fF/µm²	
Metal-1 to Poly1	C_{M1P}		0.057		fF/µm²	
Metal-1 to Silicon	C_{M1S}		0.028		fF/µm²	
Metal-2 to Metal-1	C_{MM}		0.035		fF/µm²	
Poly-1 to Poly-2	C_{P1P2}	0.69	0.86	1.03	fF/µm²	

Electrical Characteristics

NPN Bipolar Transistor Characteristics (Emitter size 4.5 x 4.5μm)

	Sym	Min	Typ	Max	Unit	Comments
Current Gain	h_{FE}		120			@100μA
Early Voltage	V_A		34		V	
Cut - Off Frequency	f_τ		1.89		GHz	
Collector-Emitter Saturation Voltage	V_{CESAT}		0.25		V	
Collector to Emitter Breakdown Voltage	BV_{CEO}	5			V	
Collector to Base Breakdown Voltage	BV_{CBO}	10			V	
Emitter to Base Breakdown Voltage	BV_{EBO}	5			V	
Emitter Resistance	R_E		30		Ω	
Base Spreading Resistance	R_B		1400		Ω	
Collector Saturation Resistance	R_C		115		Ω	
Base to Emitter Capacitance	C_{BEO}		0.102		pF	
Base to Collector Capacitance	C_{BCO}		0.041		pF	
Base to Substrate Capacitance	C_{CS}		0.125		pF	

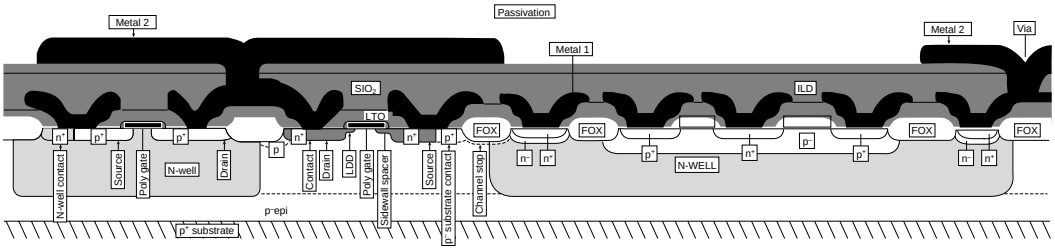
NPN Bipolar Transistor Characteristics (Emitter size 31.5 x 4.5μm)

	Sym	Min	Typ	Max	Unit	Comments
Current Gain	h_{FE}		113			@100μA
Early Voltage	V_A		34		V	
Cut - Off Frequency	f_τ		1.97		GHz	
Collector-Emitter Saturation Voltage	V_{CESAT}		0.25		V	
Collector to Emitter Breakdown Voltage	BV_{CEO}	5			V	
Collector to Base Breakdown Voltage	BV_{CBO}	10			V	
Emitter to Base Breakdown Voltage	BV_{EBO}	5			V	
Emitter Resistance	R_E		4.25		Ω	
Base Spreading Resistance	R_B		200		Ω	
Collector Saturation Resistance	R_C		16		Ω	
Base to Emitter Capacitance	C_{BEO}		0.50		pF	
Base to Collector Capacitance	C_{BCO}		0.21		pF	
Base to Substrate Capacitance	C_{CS}		0.41		pF	

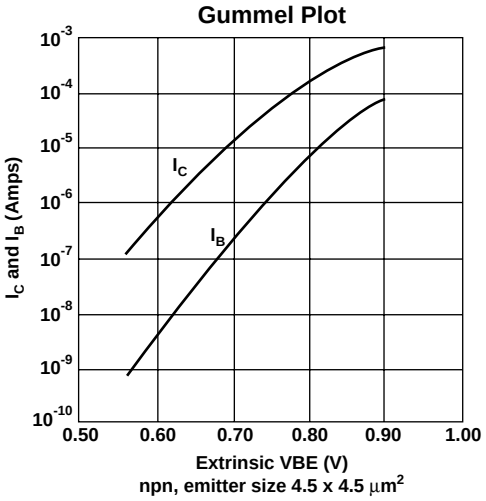
Physical Characteristics

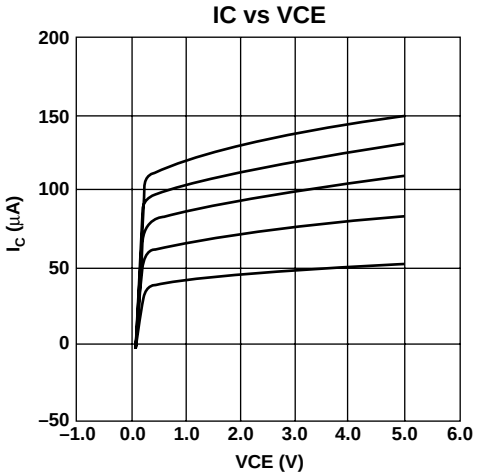
Starting Material	EPI P <100>	N+/P+ Width/Space	
Starting Mat. Resistivity	7 - 8.5 Ω-cm	N+ To P+ Space	9.0µm
Typ. Operating Voltage	5V	Contact To Poly Space	1.5µm
Well Type	N-well	Contact Overlap Of Diffusion	1.0µm
Metal Layers	2	Contact Overlap Of Poly	1.0µm
Poly Layers	2	Metal-1 Overlap Of Contact	1.0µm
Contact Size	1.5x1.5µm	Metal-1 Overlap Of Via	1.0µm
Via Size	1.5x1.5µm	Metal-2 Overlap Of Via	1.0µm
Metal-1 Width/Space	2.5 / 1.5µm	Minimum Pad Opening	65x65µm
Metal-2 Width/Space	2.5 / 1.5µm	Minimum Pad-to-Pad Spacing	5.0µm
Gate Poly Width/Space	1.5 / 2.0µm	Minimum Pad Pitch	80.0µm

Special Feature of C1203 Process: BiCMOS 1.2 µm technology with a cut-off frequency of 1.8GHz without sinkers and buried layers.



Cross-sectional view of the BICMOS 1.2 C1203 processs





Process C1206
BiCMOS 1.2µm
6.4GHz

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_N	0.55	0.75	0.95	V	100x1.2µm
Body Factor	γ_N		0.34		$V^{1/2}$	100x1.2µm
Conduction Factor	β_N	64	75	86	$\mu A/V^2$	100x100µm
Effective Channel Length	$Leff_N$	0.8	1.0	1.2	µm	100x1.2µm
Width Encroachment	ΔW_N		0.6		µm	Per side
Punch Through Voltage	$BVDSS_N$	9			V	
Poly Field Threshold Voltage	$VTF_{P(N)}$	10			V	

P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_P	–0.7	–0.9	–1.1	V	100x1.2µm
Body Factor	γ_P		0.38		$V^{1/2}$	100x1.2µm
Conduction Factor	β_P	21	25	29	$\mu A/V^2$	100x100µm
Effective Channel Length	$Leff_P$	0.9	1.1	1.3	µm	100x1.2µm
Width Encroachment	ΔW_P		0.8		µm	Per side
Punch Through Voltage	$BVDSS_P$	–9			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–10			V	

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Base Resistor Sheet Resist.	ρ_{RB}	1.33	1.66	2.00	KΩ/□	
Base Resistor Effective Width Change	ΔW_{RB}	–0.2	–0.6	–1.0	µm	
Base Resistor Voltage Coefficient, Narrow Size	V_{OLTCO_N}		11297		ppm/V	250x5µm
Base Resistor Voltage Coefficient, Wide Size	V_{OLTCO_W}		15468		ppm/V	250x25µm
Base Resistor Voltage Coefficient, Narrow Size	T_{EMPCO_N}		2761		ppm/C	250x5µm
High Resistance Poly	$\rho_{HI\text{-}POLY}$	1.5	2.0	2.5	KΩ/□	
Voltage Coefficient - High Resistance Poly	$V_{OLTCO\ HIPOLY}$	–200		0.0	ppm/V	For < 2V, 4σ 100µm
Temperature Coefficient - High Resistance Poly	$T_{EMPCO\ HIPOLY}$		–1969		ppm/C	
Base to Emitter Capacitance	C_{BEO}		33.8		$fF/\mu m^2$	
Base to Collector Cap.	C_{BCO}		56.9		$fF/\mu m^2$	
Base to Substrate Cap.	C_{CS}		35.1		$fF/\mu m^2$	
Collector to Substrate Junction Capacitance	C_{JS}		0.1		$fF/\mu m^2$	

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}	1.28	1.38	1.58	$fF/\mu m^2$	
Metal-1 to Poly-1	C_{M1P}		0.057		$fF/\mu m^2$	
Metal-1 to Silicon	C_{M1S}		0.028		$fF/\mu m^2$	
Metal-2 to Metal-1	C_{MM}		0.035		$fF/\mu m^2$	
Poly-1 to Poly-2	C_{P1P2}	0.69	0.86	1.03	$fF/\mu m^2$	

Electrical Characteristics

NPN Bipolar Transistor Characteristics (Emitter size 4.5 x 4.5μm)

	Sym	Min	Typ	Max	Unit	Comments
Current Gain	h_{FE}		102			@100μA
Early Voltage	V_A		22		V	
Cut - Off Frequency	f_τ		6.2		GHz	
Collector-Emitter Saturation Voltage	V_{CESAT}		0.25		V	
Collector to Emitter Breakdown Voltage	BV_{CEO}	5			V	
Collector to Base Breakdown Voltage	BV_{CBO}	15			V	
Emitter to Base Breakdown Voltage	BV_{EBO}	5			V	
Emitter Resistance	R_E		14		Ω	
Base Spreading Resistance	R_B		1500		Ω	
Collector Saturation Resistance	R_C		60		Ω	
Base to Emitter Capacitance	C_{BEO}		0.10		pF	
Base to Collector Capacitance	C_{BCO}		0.04		pF	
Base to Substrate Capacitance	C_{CS}		0.125		pF	

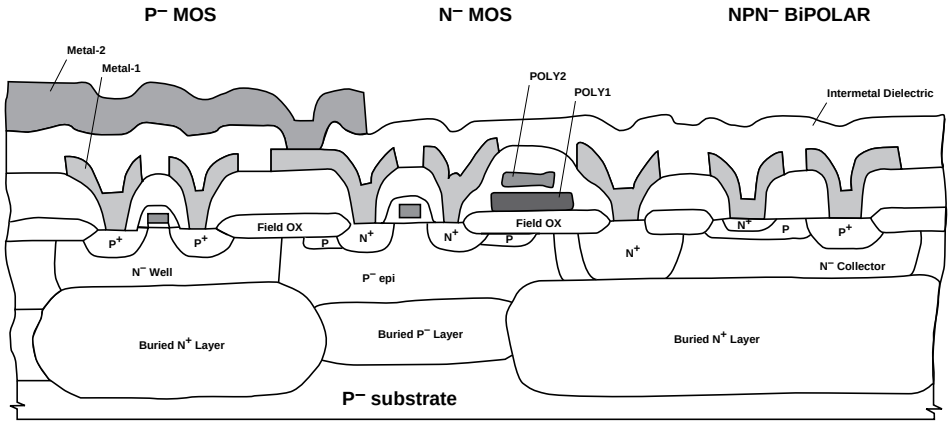
NPN Bipolar Transistor Characteristics (Emitter size 31.5 x 4.5μm)

	Sym	Min	Typ	Max	Unit	Comments
Current Gain	h_{FE}		93			@100μA
Early Voltage	V_A		22		V	
Cut - Off Frequency	f_τ		6.4		GHz	
Collector-Emitter Saturation Voltage	V_{CESAT}		0.25		V	
Collector to Emitter Breakdown Voltage	BV_{CEO}	5			V	
Collector to Base Breakdown Voltage	BV_{CBO}	15			V	
Emitter to Base Breakdown Voltage	BV_{EBO}	5			V	
Emitter Resistance	R_E		2.0		Ω	
Base Spreading Resistance	R_B		200		Ω	
Collector Saturation Resistance	R_C		10		Ω	
Base to Emitter Capacitance	C_{BEO}		0.50		pF	
Base to Collector Capacitance	C_{BCO}		0.21		pF	
Base to Substrate Capacitance	C_{CS}		0.41		pF	

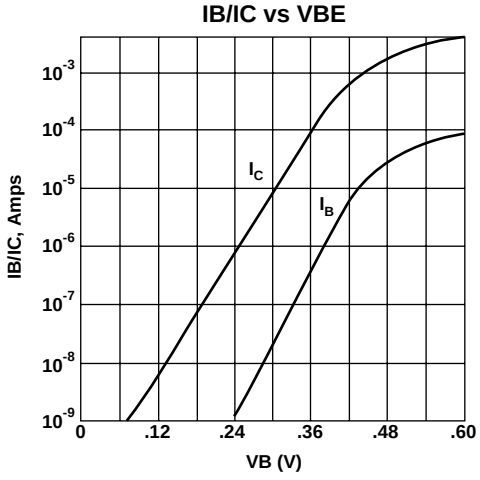
Physical Characteristics

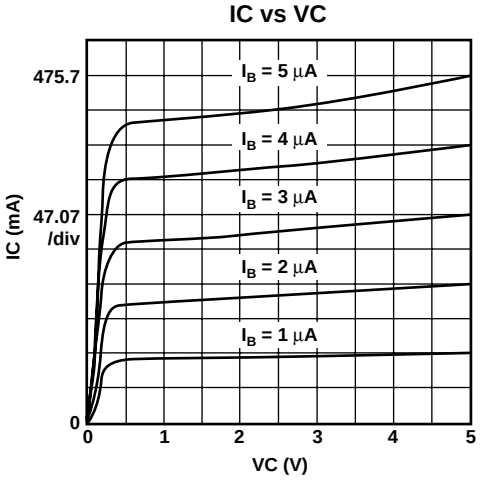
Starting Material	p <100>	N+/P+ Width/Space	2.5/1.2µm
Starting Mat. Resistivity	25 - 50 Ω-cm	N+ to P+ Space	9.0µm
Typ. Operating Voltage	5V	Contact to Poly Space	1.5µm
Well Type	N-well	Contact Overlap of Diffusion	1.0µm
Metal Layers	2	Contact Overlap of Poly	1.0µm
Poly Layers	2	Metal-1 Overlap of Contact	1.0µm
Contact Size	1.5x1.5µm	Metal-1 Overlap of Via	1.0µm
Via Size	1.5x1.5µm	Metal-2 Overlap of Via	1.0µm
Metal-1 Width/Space	2.5 / 1.5µm	Minimum Pad Opening	65x65µm
Metal-2 Width/space	2.5 / 1.5µm	Minimum Pad-to-Pad Spacing	5.0µm
Gate Poly Width/Space	1.5 / 2.0µm	Minimum Pad Pitch	80.0µm

Special feature of C1206 Process: BiCMOS 1.2-µm technology with a cutoff frequency of 6.4GHz.



Cross-sectional view of the BiCMOS 1.2 C1206 process





Process C1209
1.2µm EECMOS

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_N	0.55	0.75	0.95	V	100x1.2µm
Body Factor	γ_N		0.34		$V^{1/2}$	100x1.2µm
Conduction Factor	β_N	64	75	86	µA/V²	100/100µm
Effective Channel Length	$Leff_N$	0.8	1.0	1.2	µm	100x1.2µm
Width Encroachment	ΔW_N		0.6		µm	Per side
Punch Through Voltage	$BVDSS_N$	9			V	
Poly Field Threshold	$VTF_{P(N)}$	10	16		V	

N-Channel Native Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_{ZBN}		0.310		V	100x2.5µm
Body Factor	γ_{ZBN}		0.45		$V^{1/2}$	100x1.2µm
Conduction Factor	β_{ZBN}		55		µA/V²	100/100µm

P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_P	–0.7	–0.9	–1.1	V	100x1.2µm
Body Factor	γ_P		0.38		$V^{1/2}$	100x1.2µm
Conduction Factor	β_P	21	25	29	µA/V²	100/100µm
Effective Channel Length	$Leff_P$	0.9	1.1	1.3	µm	100x1.2µm
Width Encroachment	ΔW_P		0.8		µm	Per side
Punch Through Voltage	$BVDSS_P$	–9			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–10	–20		V	

EECMOS Characteristics	Symbol	Minimum	Typical	Maximum	Unit	Comments
Tunnel Oxide Thickness	T_{TUNLOX}		90		A	
Interpoly Oxide Thickness	T_{P1P2}		400		A	
Buried N+ Sheet Res.	ρ_{BN+}		200		Ω/□	
Initial Program/Erase Window			5		V	
Erased Memory Threshold	V_T		–1.7		V	
Endurance			10,000		Cycles	
Programming Voltage	VPP		13		V	
Programmed Threshold			3		V	
SIngle Cell Size			30x15		µm²	
256-Bit Memory Size			1450x543		µm²	

Electrical Characteristics

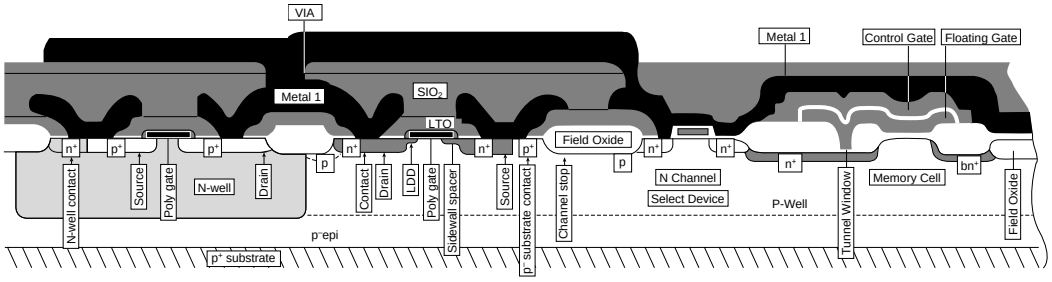
Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{N\text{-}well(f)}$	0.6	1.0	1.3	KΩ/□	n-well
N+ Sheet Resistance	ρ_{N+}	20	35	50	Ω/□	
N+ Junction Depth	x_{jN+}		0.35		µm	
P+ Sheet Resistance	ρ_{P+}	50	75	100	Ω/□	
P+ Junction Depth	x_{jP+}		0.35		µm	
Gate Oxide Thickness	T_{GOX}		24		nm	
Field Oxide Thickness	T_{FIELD}		800		nm	
Gate Poly Sheet Res.	ρ_{POLY2}	15	22	30	Ω/□	
Bottom Poly Sheet Res.	ρ_{POLY1}		35		Ω/□	
Metal-1 Sheet Resistance	ρ_{M1}		50		mΩ/□	
Metal-2 Sheet Resistance	ρ_{M2}		30		mΩ/□	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}	1.28	1.38	1.58	fF/µm²	
Metal-1 to Poly1	C_{M1P}		0.057		fF/µm²	
Metal-1 to Silicon	C_{M1S}		0.028		fF/µm²	
Metal-2 to Metal-1	C_{MM}		0.035		fF/µm²	
Poly-1 to Poly-2	C_{P1P2}		0.86		fF/µm²	

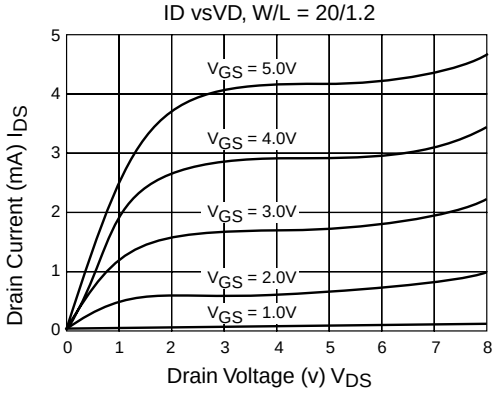
Physical Characteristics

Starting Material	EPI P <100>	N+/P+ Width/Space	2.5 / 2.0µm
Starting Mat. Resistivity	7 - 8.5 Ω-cm	N+ To P+ Space	9.0µm
Typ. Operating Voltage	5V	Contact To Poly Space	1.5µm
Well Type	N-well	Contact Overlap Of Diffusion	1.0µm
Metal Layers	2	Contact Overlap Of Poly	1.0µm
Poly Layers	2	Metal-1 Overlap Of Contact	1.0µm
Contact Size	1.5x1.5µm	Metal-1 Overlap Of Via	1.0µm
Via Size	1.5x1.5µm	Metal-2 Overlap Of Via	1.0µm
Metal-1 Width/Space	2.5 / 1.5µm	Minimum Pad Opening	65x65µm
Metal-2 Width/Space	2.5 / 1.5µm	Minimum Pad-to-Pad Spacing	5.0µm
Gate Poly Width/Space	1.5 / 2.0µm	Minimum Pad Pitch	80.0µm

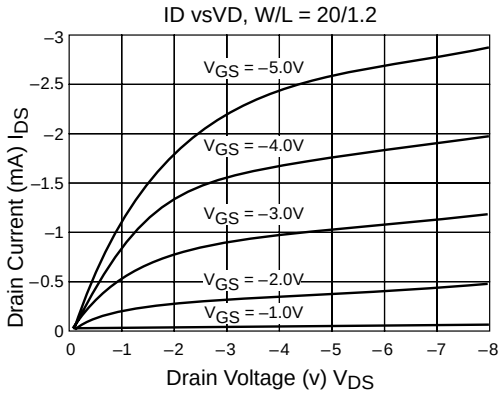
Special Feature of C1209 Process: EECMOS technology with analog capacitors and zero threshold n-channel transistors.



Cross-sectional view of the EECMOS 1.2 process



n-ch Transistor IV characteristics of a 20/1.2 device



p-ch Transistor IV characteristics of a 20/1.2 device

Process C1210
CMOS 1.2µm
Zero Threshold Devices

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_N	0.55	0.75	0.95	V	100x1.2µm
Body Factor	γ_N		0.34		$V^{1/2}$	100x1.2µm
Conduction Factor	β_N	64	75	86	µA/V²	100x100µm
Effective Channel Length	$Leff_N$	0.8	1.0	1.2	µm	100x1.2µm
Width Encroachment	ΔW_N		0.6		µm	Per side
Punch Through Voltage	$BVDSS_N$	9			V	
Poly Field Threshold Voltage	$VTF_{P(N)}$	10			V	

Zero Vt N-Channel Transis.	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_{ZLN}	0.00	0.15	0.30	V	100x100µm
Body Factor	γ_{ZLN}		0.348		$V^{1/2}$	100x100µm
Conduction Factor	β_{ZLN}	75	90	105	µA/V²	100x100µm
Saturation Current	I_{DSATZN}	28	34	40	mA	100x1.5µm

P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_P	–0.7	–0.9	–1.1	V	100x1.2µm
Body Factor	γ_P		0.38		$V^{1/2}$	100x1.2µm
Conduction Factor	β_P	21	25	29	µA/V²	100x100µm
Effective Channel Length	$Leff_P$	0.9	1.1	1.3	µm	100x1.2µm
Width Encroachment	ΔW_P		0.8		µm	Per side
Punch Through Voltage	$BVDSS_P$	–9.0			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–10.0			V	

Zero Vt P-Channel Transis.	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_{ZLP}	–0.3	–0.1	0.1	V	100x100µm
Body Factor	γ_{ZLP}		0.36		$V^{1/2}$	100x100µm
Conduction Factor	β_{ZLP}	21	26	31	µA/V²	100x100µm
Saturation Current	I_{DSATZP}	–11	–15	–19	mA	100x1.5µm

Electrical Characteristics

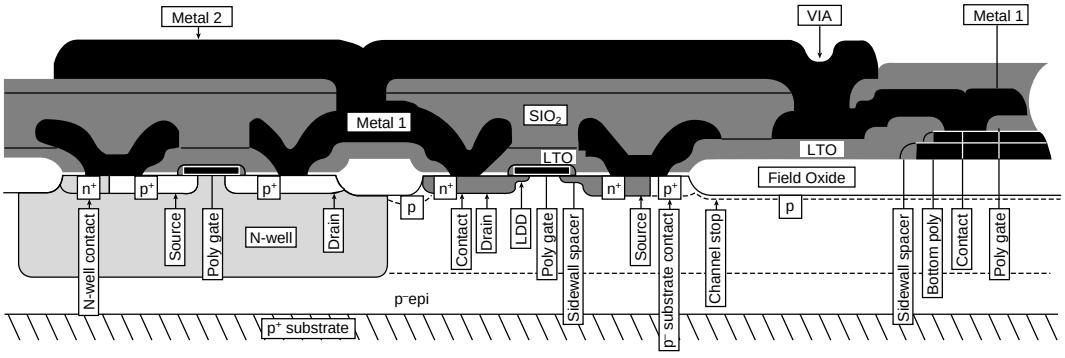
Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{N\text{-}well(f)}$	0.6	1.0	1.3	KΩ/□	n-well
N+ Sheet Resistance	ρ_{N+}	20	35	50	Ω/□	
N+ Junction Depth	x_{jN+}		0.35		µm	
P+ Sheet Resistance	ρ_{P+}	50	75	100	Ω/□	
P+ Junction Depth	x_{jP+}		0.35		µm	
Gate Oxide Thickness	T_{GOX}		24		nm	
Field Oxide Thickness	T_{FIELD}		800		nm	
Gate Poly Sheet Resistance	ρ_{POLY2}	15	22	30	Ω/□	
Bottom Poly Sheet Res.	ρ_{POLY1}		35		Ω/□	
Metal-1 Sheet Resistance	ρ_{M1}		50		mΩ/□	
Metal-2 Sheet Resistance	ρ_{M2}		30		mΩ/□	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}	1.28	1.38	1.58	fF/µm²	
Metal-1 to Poly-1	C_{M1P}		0.057		fF/µm²	
Metal-1 to Silicon	C_{M1S}				fF/µm²	
Metal-2 to Metal-1	C_{MM}		0.035		fF/µm²	
Poly-1 to Poly-2	C_{P1P2}	0.69	0.86	1.03	fF/µm²	

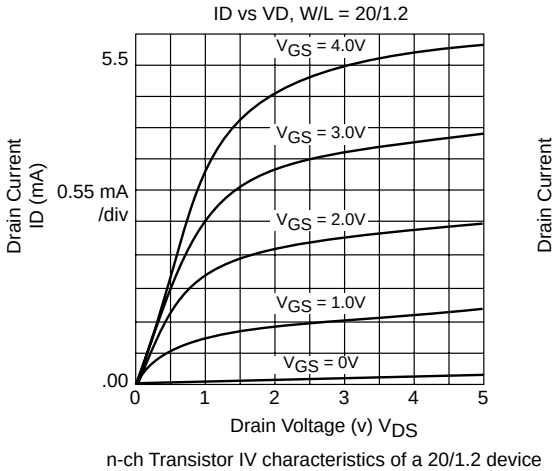
Physical Characteristics

Starting Material	EPI P <100>	N+/P+ Width/Space	2.5/ 2.0µm
Starting Mat. Resistivity	7 - 8.5 Ω-cm	N+ To P+ Space	9.0µm
Typ. Operating Voltage	5V	Contact To Poly Space	1.5µm
Well Type	N-well	Contact Overlap Of Diffusion	1.0µm
Metal Layers	2	Contact Overlap Of Poly	1.0µm
Poly Layers	2	Metal-1 Overlap Of Contact	1.0µm
Contact Size	1.5x1.5µm	Metal-1 Overlap Of Via	1.0µm
Via Size	1.5x1.5µm	Metal-2 Overlap Of Via	1.0µm
Metal-1 Width/Space	2.5 / 1.5µm	Minimum Pad Opening	65x65µm
Metal-2 Width/Space	2.5 / 1.5µm	Minimum Pad-to-Pad Spacing	5.0µm
Gate Poly Width/Space	1.5 / 2.0µm	Minimum Pad Pitch	80.0µm

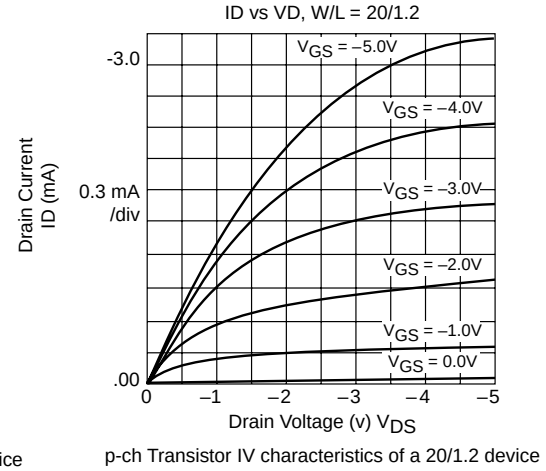
Special Feature of C1210 Process: This process offers zero threshold n- and p-channel transistors in addition to normal threshold transistors of CMOS 1.2µm technology.



Cross-Sectional view of the LVMOS process



n-ch Transistor IV characteristics of a 20/1.2 device



p-ch Transistor IV characteristics of a 20/1.2 device

Process C1212
BiCMOS 1.2µm
12 Volt Bipolar Operation

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_N	0.55	0.75	0.95	V	100x1.2µm
Body Factor	γ_N		0.34		$V^{1/2}$	100x1.2µm
Conduction Factor	β_N	64	75	86	µA/V²	100x100µm
Effective Channel Length	$Leff_N$	0.8	1.0	1.2	µm	100x1.2µm
Width Encroachment	ΔW_N		0.6		µm	Per side
Punch Through Voltage	$BVDSS_N$	9			V	
Poly Field Threshold Voltage	$VTF_{P(N)}$	10			V	

P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_P	–0.7	–0.9	–1.1	V	100x1.2µm
Body Factor	γ_P		0.38		$V^{1/2}$	100x1.2µm
Conduction Factor	β_P	21	25	29	µA/V²	100x100µm
Effective Channel Length	$Leff_P$	0.9	1.1	1.3	µm	100x1.2µm
Width Encroachment	ΔW_P		0.8		µm	Per side
Punch Through Voltage	$BVDSS_P$	–9			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–10			V	

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{N\text{-well(f)}}$	0.6	1.0	1.3	KΩ/□	n-well
N+ Sheet Resistance	ρ_{N+}	20	35	50	Ω/□	
N+ Junction Depth	x_{jN+}		0.35		µm	
P+ Sheet Resistance	ρ_{P+}	50	75	100	Ω/□	
P+ Junction Depth	x_{jP+}		0.35		µm	
Gate Oxide Thickness	T_{GOX}		24		nm	
Field Oxide Thickness	T_{FIELD}		800		nm	
Gate Poly Sheet Resistance	ρ_{POLY2}	15	22	30	Ω/□	
Bottom Poly Sheet Res.	ρ_{POLY1}		35		Ω/□	
Metal-1 Sheet Resistance	ρ_{M1}		50		mΩ/□	
Metal-2 Sheet Resistance	ρ_{M2}		30		mΩ/□	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}	1.28	1.38	1.58	fF/µm²	
Metal-1 to Poly-1	C_{M1P}		0.057		fF/µm²	
Metal-1 to Silicon	C_{M1S}		0.028		fF/µm²	
Metal-2 to Metal-1	C_{MM}		0.035		fF/µm²	
Poly-1 to Poly-2	C_{P1P2}	0.69	0.86	1.03	fF/µm²	

Electrical Characteristics

NPN Bipolar Transistor Characteristics (Emitter size 4.5 x 4.5μm)

	Sym	Min	Typ	Max	Unit	Comments
Current Gain	h_{FE}		105			@5μA
Early Voltage	V_A		22		V	
Cut - Off Frequency	f_τ		6.2		GHz	
Collector-Emitter Saturation Voltage	V_{CESAT}		0.33		V	
Collector to Emitter Breakdown Voltage	BV_{CEO}	14			V	
Collector to Base Breakdown Voltage	BV_{CBO}	27			V	
Emitter to Base Breakdown Voltage	BV_{EBO}	6			V	
Emitter Resistance	R_E		40		Ω	
Base Spreading Resistance	R_B		500		Ω	
Collector Saturation Resistance	R_C		100		Ω	
Base to Emitter Capacitance	C_{BEO}		0.10		pF	
Base to Collector Capacitance	C_{BCO}		0.04		pF	
Base to Substrate Capacitance	C_{CS}		0.125		pF	

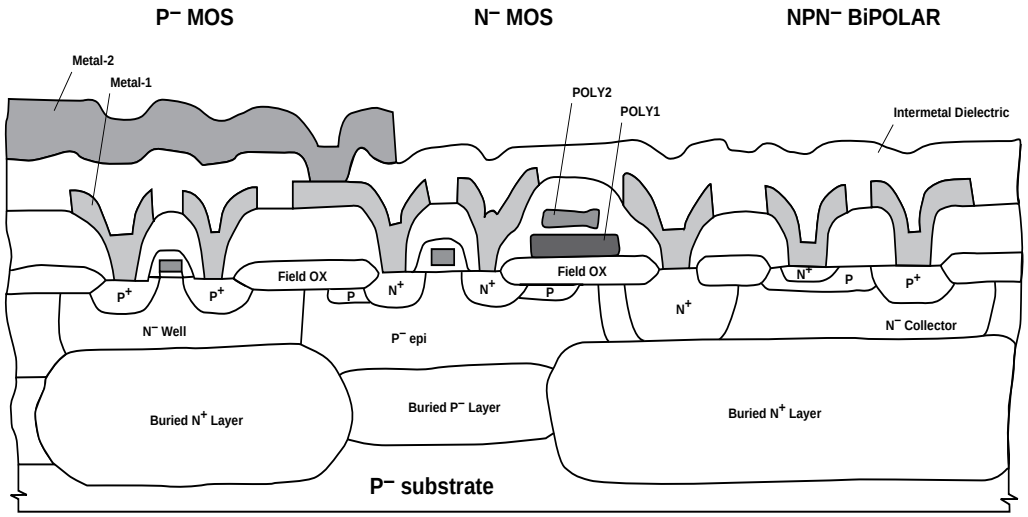
NPN Bipolar Transistor Characteristics (Emitter size 31.5 x 4.5μm)

	Sym	Min	Typ	Max	Unit	Comments
Current Gain	h_{FE}		115			@5μA
Early Voltage	V_A		22		V	
Cut - Off Frequency	f_τ		6.4		GHz	
Collector-Emitter Saturation Voltage	V_{CESAT}		0.38		V	
Collector to Emitter Breakdown Voltage	BV_{CEO}	6			V	
Collector to Base Breakdown Voltage	BV_{CBO}	27			V	
Emitter to Base Breakdown Voltage	BV_{EBO}	14			V	
Emitter Resistance	R_E		6		Ω	
Base Spreading Resistance	R_B		100		Ω	
Collector Saturation Resistance	R_C		15		Ω	
Base to Emitter Capacitance	C_{BEO}		0.10		pF	
Base to Collector Capacitance	C_{BCO}		0.04		pF	
Base to Substrate Capacitance	C_{CS}		0.125		pF	

Physical Characteristics

Starting Material	P <100>	N+/P+ Width/Space	2.5 / 2.0µm
Starting Mat. Resistivity	25 - 50 Ω-cm	N+ To P+ Space	9.0µm
Typ. Operating Voltage	5V	Contact To Poly Space	1.5µm
Well Type	N-well	Contact Overlap Of Diffusion	1.0µm
Metal Layers	2	Contact Overlap Of Poly	1.0µm
Poly Layers	2	Metal-1 Overlap Of Contact	1.0µm
Contact Size	1.5x1.5µm	Metal-1 Overlap Of Via	1.0µm
Via Size	1.5x1.5µm	Metal-2 Overlap Of Via	1.0µm
Metal-1 Width/Space	2.5 / 1.5µm	Minimum Pad Opening	65x65µm
Metal-2 Width/Space	2.5 / 1.5µm	Minimum Pad-to-Pad Spacing	5.0µm
Gate Poly Width/Space	1.5 / 2.0µm	Minimum Pad Pitch	80.0µm

Special Feature of C1212 Process: BiCMOS 1.2µm technology with a cut-off frequency of 6.4GHz and Bipolar operating voltage up to 12Volts.



Cross-scetional view of the BiCMOS 1.2 process

Process C1215
CMOS 1.2µm
Low Threshold Devices

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_N	0.3	0.475	0.65	V	100x1.2µm
Body Factor	γ_N	0.29	0.36	0.44	$V^{1/2}$	100x1.2µm
Conduction Factor	β_N	75	90	105	$\mu A/V^2$	100x100µm
Effective Channel Length	$Leff_N$	0.8	1.0	1.2	µm	100x1.2µm
Width Encroachment	ΔW_N		0.6		µm	Per side
Punch Through Voltage	$BVDSS_N$	9			V	
Poly Field Threshold Voltage	$VTF_{P(N)}$	10			V	

P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_P	–0.3	–0.475	–0.65	V	100x1.2µm
Body Factor	γ_P	0.4	0.5	0.7	$V^{1/2}$	100x1.2µm
Conduction Factor	β_P	18	23	28	$\mu A/V^2$	100x100µm
Effective Channel Length	$Leff_P$	0.9	1.1	1.3	µm	100x1.2µm
Width Encroachment	ΔW_P		0.8		µm	Per side
Punch Through Voltage	$BVDSS_P$	–9.0			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–10.0			V	

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{N\text{-well(f)}}$	0.8	1.4	2.0	KΩ/□	n-well
N+ Sheet Resistance	ρ_{N+}	20	35	50	Ω/□	
N+ Junction Depth	x_{jN+}		0.35		µm	
P+ Sheet Resistance	ρ_{P+}	50	75	100	Ω/□	
P+ Junction Depth	x_{jP+}		0.35		µm	
Gate Oxide Thickness	T_{GOX}		24		nm	
Field Oxide Thickness	T_{FIELD}		800		nm	
Gate Poly Sheet Resistance	ρ_{POLY1}	15	22	30	Ω/□	
Top Poly Sheet Reistance	ρ_{POLY2}		35		Ω/□	
Metal-1 Sheet Resistance	ρ_{M1}		50		mΩ/□	
Metal-2 Sheet Resistance	ρ_{M2}		30		mΩ/□	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}	1.28	1.38	1.58	$fF/\mu m^2$	
Metal-1 to Poly-1	C_{M1P}		0.046		$fF/\mu m^2$	
Metal-1 to Silicon	C_{M1S}		0.028		$fF/\mu m^2$	
Metal-2 to Metal-1	C_{MM}		0.035		$fF/\mu m^2$	
Poly-1 to Poly-2	C_{P1P2}	0.69	0.86	1.03	$fF/\mu m^2$	

Physical Characteristics

Starting Material	P <100>	N+/P+ Width/Space	2.5 / 2.0µm
Starting Mat. Resistivity	25 - 50 Ω-cm	N+ To P+ Space	9.0µm
Max Operating Voltage	3V-5V	Contact To Poly Space	1.5µm
Well Type	N-well	Contact Overlap Of Diffusion	1.0µm
Metal Layers	2	Contact Overlap Of Poly	1.0µm
Poly Layers	2	Metal-1 Overlap Of Contact	1.0µm
Contact Size	1.5x1.5µm	Metal-1 Overlap Of Via	1.0µm
Via Size	1.5x1.5µm	Metal-2 Overlap Of Via	1.0µm
Metal-1 Width/Space	2.5 / 1.5µm	Minimum Pad Opening	65x65µm
Metal-2 Width/Space	2.5 / 1.5µm	Minimum Pad-to-Pad Spacing	5.0µm
Gate Poly Width/Space	1.5 / 2.0µm	Minimum Pad Pitch	80.0µm

Special Feature of C1215 Process: Low threshold n- and p-channel transistors in CMOS 1.2 µm technology.

Process C1216
CMOS 1.2µm
15 Volt Operation

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_N	0.75	0.95	1.15	V	100x1.5µm
Body Factor	γ_N		0.81		$V^{1/2}$	100x1.5µm
Conduction Factor	β_N	37	46	55	$\mu A/V^2$	100x100µm
Effective Channel Length	$Leff_N$		1.35	2	µm	100x1.5µm
Width Encroachment	ΔW_N		0.665		µm	Per side
Punch Through Voltage	$BVDSS_N$	18	21		V	
Poly Field Threshold Voltage	$VTF_{P(N)}$	18	20		V	

P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_P	–0.80	–1.00	–1.20	V	100x1.2µm
Body Factor	γ_P		0.65		$V^{1/2}$	100x1.2µm
Conduction Factor	β_P	11	15	20	$\mu A/V^2$	100x100µm
Effective Channel Length	$Leff_P$		1.5		µm	100x1.2µm
Width Encroachment	ΔW_P		0.7		µm	Per side
Punch Through Voltage	$BVDSS_P$	–18	–21		V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–18	–20		V	

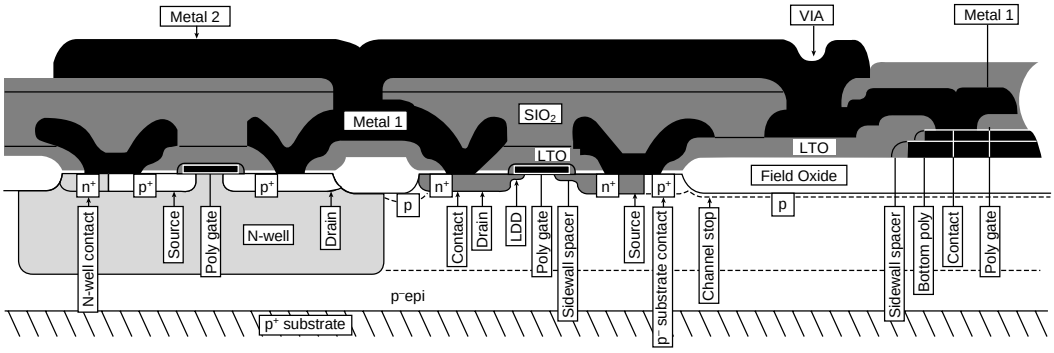
Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{N\text{-well(f)}}$	1.4	1.8	2.2	KΩ/□	n-well
N-well Junction Depth	X_{JNWELL}		3.0		µm	
N+ Sheet Resistance	ρ_{N+}	20	35	50	Ω/□	
N+ Junction Depth	x_{jN+}		0.6		µm	
P+ Sheet Resistance	ρ_{P+}	50	75	100	Ω/□	
P+ Junction Depth	x_{jP+}		0.4		µm	
Gate Oxide Thickness (HV)	T_{GOX}		48		nm	
Field Oxide Thickness	T_{FIELD}		1000		nm	
Gate Poly Sheet Resistance	ρ_{POLY2}	15	22	30	Ω/□	
Bottom Poly Sheet Res.	ρ_{POLY1}	20	25	30	Ω/□	
Metal-1 Sheet Resistance	ρ_{M1}		42		mΩ/□	
Metal-2 Sheet Resistance	ρ_{M2}	19	25	32	mΩ/□	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}		0.719		$fF/\mu m^2$	
Metal-1 to Poly-1	C_{M1P}		0.046		$fF/\mu m^2$	
Metal-1 to Silicon	C_{M1S}		0.028		$fF/\mu m^2$	
Metal-2 to Metal-1	C_{MM}		0.050		$fF/\mu m^2$	
Poly-1 to Poly-2	C_{P1P2}	0.69	0.86	1.03	$fF/\mu m^2$	

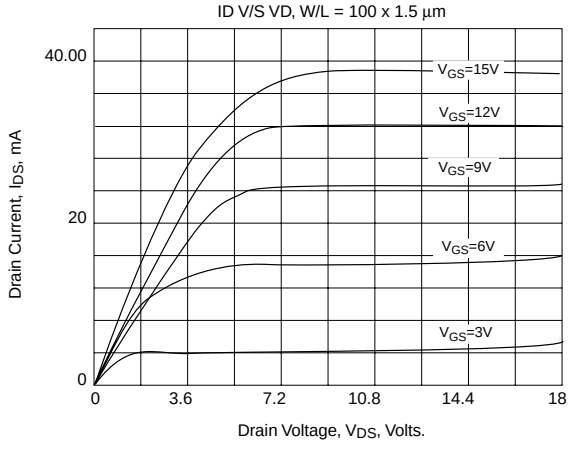
Physical Characteristics

Starting Material	P <100>	N+/P+ Width/Space	2.5 / 2.0µm
Starting Mat. Resistivity	4 - 6.6 Ω-cm	N+ To P+ Space	9.0µm
Operating Voltage	15V	Contact To Poly Space	1.5µm
Well Type	N-well	Contact Overlap Of Diffusion	1.0µm
Metal Layers	2	Contact Overlap Of Poly	1.0µm
Poly Layers	2	Metal-1 Overlap Of Contact	1.0µm
Contact Size	1.5x1.5µm	Metal-1 Overlap Of Via	1.0µm
Via Size	1.5x1.5µm	Metal-2 Overlap Of Via	1.0µm
Metal-1 Width/Space	2.5 / 1.5µm	Minimum Pad Opening	65x65µm
Metal-2 Width/Space	2.5 / 1.5µm	Minimum Pad-to-Pad Spacing	5.0µm
Gate Poly Width/Space	1.5 / 2.0µm	Minimum Pad Pitch	80.0µm

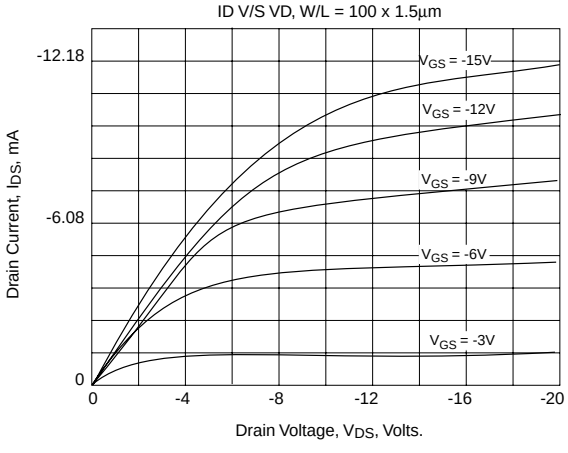
Special Feature of C1216 Process: 15 Volt operating n- and p-channel transistors are available along with 5 Volt CMOS 1.2 µm devices.



Similar structures with offset source/drain for 15V devices



n - Channel Transistor Characteristics



P - Channel Transistor Characteristics

Process C1219
CMOS 1.2μm
EEPROM

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_N	0.30	0.475	0.65	V	100x10μm
Body Factor	γ_N	0.35	0.45	0.55	$V^{1/2}$	100x100μm
Conduction Factor	β_N	64	78	92	$\mu A/V^2$	100x100μm
Saturation Current	I_{DSATN}	16	25	40	mA	100x1.5μm
Punch Through Voltage	$BVDSS_N$	5			V	
Poly Field Threshold	$VTF_{P(N)}$	8			V	

N-Channel Native Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_{ZBN}	−0.20	0.37	0.52	V	100x2.5μm
Body Factor	γ_{ZBN}	0.30	0.45	0.60	$V^{1/2}$	100x2.5μm
Saturation Current	I_{DSATN}	13	15.7	18.9	mA	100x2.5μm
Conduction Factor	β_{ZBN}	45	55	65	$\mu A/V^2$	100x100μm

P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_P	−0.65	−0.475	−0.30	V	100x1.2μm
Body Factor	γ_P	0.5	0.6	0.7	$V^{1/2}$	100x1.2μm
Conduction Factor	β_P	20	25	30	$\mu A/V^2$	100x100μm
Saturation Current	I_{DSATP}	−6	−10	−16	mA	100x1.5μm
Punch Through Voltage	$BVDSS_P$	−5			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	−8			V	

EECMOS Characteristics	Symbol	Minimum	Typical	Maximum	Unit	Comments
Tunnel Oxide Thickness	T_{TUNLOX}	84	88	92	nm	
Interpoly Oxide Thickness	T_{P1P2}	340	390	440	nm	
Buried N+ Sheet Res.	ρ_{BN+}	200	300	400	Ω/□	
Initial Program/Erase Window			3.0		V	
Unprog. Memory Threshold	V_T		3.0		V	
Endurance		10,000			Cycles	
Programming Voltage	VPP	12	14	17	V	

Electrical Characteristics

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{N\text{-well(f)}}$	1.2	2.0	2.8	KΩ/□	n-well
N+ Sheet Resistance	ρ_{N+}	20	35	50	Ω/□	
N+ Junction Depth	x_{jN+}		0.35		µm	
P+ Sheet Resistance	ρ_{P+}	60	110	160	Ω/□	
P+ Junction Depth	x_{jP+}		0.35		µm	
Gate Oxide Thickness	T_{GOX}	22.5	25.0	27.5	nm	
Field Oxide Thickness	T_{FIELD}		700		nm	
Gate Poly Sheet Res.	ρ_{POLY2}	25	35	45	Ω/□	
Bottom Poly Sheet Res.	ρ_{POLY1}	24	32	40	Ω/□	
High Resistance Poly	ρ_{POLYHI}	1.5	2.0	2.5	kΩ/□	
Metal-1 Sheet Resistance	ρ_{M1}		50		mΩ/□	
Metal-2 Sheet Resistance	ρ_{M2}	19	25	32	mΩ/□	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}	1.28	1.38	1.58	fF/µm²	
Metal-1 to Poly1	C_{M1P}		0.057		fF/µm²	
Metal-1 to Silicon	C_{M1S}		0.028		fF/µm²	
Metal-2 to Metal-1	C_{MM}		0.035		fF/µm²	
Poly-1 to Poly-2	C_{P1P1}		0.86		fF/µm²	

Physical Characteristics

Starting Material	EPI P <100>	N+/P+ Width/Space	2.0 / 2.0µm
Starting Mat. Resistivity	7 - 8.5 Ω-cm	N+ To P+ Space	9.0µm
Operating Voltage	5V	Tunnel Oxide Width/Space	1.5 / 1.5µm
Well Type	N-well	Tunnel Ox. Overlap Bot. Poly	1.0µm
Metal Layers	2	Contact To Poly Space	1.5µm
Poly Layers	2	Contact Overlap Of Diffusion	1.0µm
Contact Size	1.5x1.5µm	Contact Overlap Of Poly	1.0µm
Via Size	1.5x1.5µm	Metal-1 Overlap Of Contact	1.0µm
Metal-1 Width/Space	2.5 / 1.5µm	Metal-1 Overlap Of Via	1.0µm
Metal-2 Width/Space	2.5 / 1.5µm	Metal-2 Overlap Of Via	1.0µm
Gate Poly Width/Space	1.5 / 2.0µm	Minimum Pad Opening	65x65µm
Buried N+ Width/Space	2.5 / 1.75µm	Minimum Pad-to-Pad Spacing	5.0µm
High Poly Width/Space	1.5 / 1.5µm	Minimum Pad Pitch	80.0µm

Special Feature of C1219 Process: EEPROM process with high resistivity poly resistors and native n-channel devices.

Process C1221

BiCMOS 1.2µm

High Resistance Poly for Analog

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_N	0.55	0.75	0.95	V	100x1.2µm
Body Factor	γ_N		0.34		$V^{1/2}$	100x1.2µm
Conduction Factor	β_N	64	75	86	µA/V²	100x100µm
Effective Channel Length	$Leff_N$	0.8	1.0	1.2	µm	100x1.2µm
Width Encroachment	ΔW_N		0.6		µm	Per side
Punch Through Voltage	$BVDSS_N$	9			V	
Poly Field Threshold Voltage	$VTF_{P(N)}$	10			V	

P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_P	–0.7	–0.9	–1.1	V	100x1.2µm
Body Factor	γ_P		0.38		$V^{1/2}$	100x1.2µm
Conduction Factor	β_P	21	25	29	µA/V²	100x100µm
Effective Channel Length	$Leff_P$	0.9	1.1	1.3	µm	100x1.2µm
Width Encroachment	ΔW_P		0.8		µm	Per side
Punch Through Voltage	$BVDSS_P$	–9			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–10			V	

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Base Resistor Sheet Resist.	ρ_{RB}	1.33	1.66	2.00	KΩ/□	
Base Resistor Effective Width Change	ΔW_{RB}	–0.2	–0.6	–1.0	µm	
Base Resistor Voltage Coefficient, Narrow Size	$VOLTCO_N$		11297		ppm/V	250x5µm
Base Resistor Voltage Coefficient, Wide Size	$VOLTCO_W$		15468		ppm/V	250x25µm
Base Resistor Voltage Coefficient, Narrow Size	$TEMPCO_N$		2761		ppm/C	250x5µm
High Resistance Poly	$\rho_{HI\text{-}POLY}$	1.5	2.0	2.5	KΩ/□	
Voltage Coefficient - High Resistance Poly	$VOLTCO_{HIPOLY}$	–200		0.0	ppm/V	For < 2V, 4σ 100µm
Temperature Coefficient - High Resistance Poly	$TEMPCO_{HIPOLY}$		–1969		ppm/C	
Base to Emitter Capacitance	C_{BEO}		33.8		fF/µm²	
Base to Collector Cap.	C_{BCO}		56.9		fF/µm²	
Base to Substrate Cap.	C_{CS}		35.1		fF/µm²	
Collector to Substrate Junction Capacitance	C_{JS}		0.1		fF/µm²	

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}	1.28	1.38	1.58	fF/µm²	
Metal-1 to Poly-1	C_{M1P}		0.057		fF/µm²	
Metal-1 to Silicon	C_{M1S}		0.028		fF/µm²	
Metal-2 to Metal-1	C_{MM}		0.035		fF/µm²	
Poly-1 to Poly-2	C_{P1P2}	0.69	0.86	1.03	fF/µm²	

Electrical Characteristics

NPN Bipolar Transistor Characteristics (Emitter size 4.5 x 4.5μm)

	Sym	Min	Typ	Max	Unit	Comments
Current Gain	h_{FE}		118			@100μA
Early Voltage	V_A		22		V	
Cut - Off Frequency	f_τ		6.2		GHz	
Collector-Emitter Saturation Voltage	V_{CESAT}		0.3		V	
Collector to Emitter Breakdown Voltage	BV_{CEO}		6.5		V	
Collector to Base Breakdown Voltage	BV_{CBO}		17		V	
Emitter to Base Breakdown Voltage	BV_{EBO}		6		V	
Emitter Resistance	R_E		40		Ω	
Base Spreading Resistance	R_B		1000		Ω	
Collector Saturation Resistance	R_C		100		Ω	
Base to Emitter Capacitance	C_{BEO}				pF	
Base to Collector Capacitance	C_{BCO}				pF	
Base to Substrate Capacitance	C_{CS}				pF	

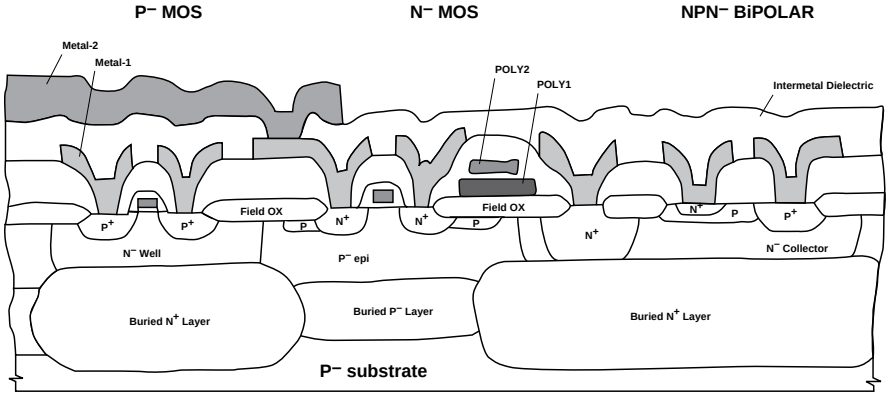
NPN Bipolar Transistor Characteristics (Emitter size 31.5 x 4.5μm)

	Sym	Min	Typ	Max	Unit	Comments
Current Gain	h_{FE}		110			@100μA
Early Voltage	V_A		22		V	
Cut - Off Frequency	f_τ		6.4		GHz	
Collector-Emitter Saturation Voltage	V_{CESAT}		0.2		V	
Collector to Emitter Breakdown Voltage	BV_{CEO}		6.5		V	
Collector to Base Breakdown Voltage	BV_{CBO}		17		V	
Emitter to Base Breakdown Voltage	BV_{EBO}		6		V	
Emitter Resistance	R_E		6		Ω	
Base Spreading Resistance	R_B		250		Ω	
Collector Saturation Resistance	R_C		15		Ω	

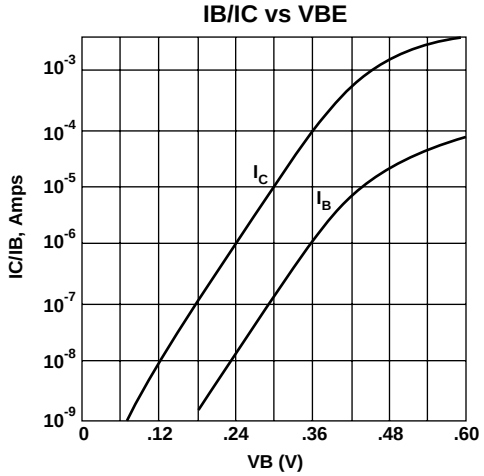
Physical Characteristics

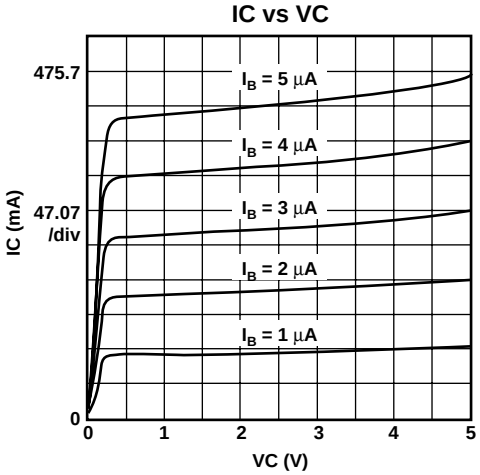
Starting Material	p <100>	N+/P+ Width/Space	2.5/1.2µm
Starting Mat. Resistivity	25 - 50 Ω-cm	N+ to P+ Space	9.0µm
Typ. Operating Voltage	5V	Contact to Poly Space	1.5µm
Well Type	N-well	Contact Overlap of Diffusion	1.0µm
Metal Layers	2	Contact Overlap of Poly	1.0µm
Poly Layers	2	Metal-1 Overlap of Contact	1.0µm
Contact Size	1.5x1.5µm	Metal-1 Overlap of Via	1.0µm
Via Size	1.5x1.5µm	Metal-2 Overlap of Via	1.0µm
Metal-1 Width/Space	2.5 / 1.5µm	Minimum Pad Opening	65x65µm
Metal-2 Width/space	2.5 / 1.5µm	Minimum Pad-to-Pad Spacing	5.0µm
Gate Poly Width/Space	1.5 / 2.0µm	Minimum Pad Pitch	80.0µm

Special feature of C1206 Process: BiCMOS 1.2-µm technology with a cutoff frequency of 6.4GHz.



Cross-sectional view of the BiCMOS 1.2 C1221 process





Process C1225
1.2µm BiCMOS

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_N	0.45	0.65	0.85	V	100x1.2µm
Body Factor	γ_N	0.45	0.60	0.85	$V^{1/2}$	100x1.2µm
Conduction Factor	β_N	60	77	95	$\mu A/V^2$	100x100µm
Effective Channel Length	$Leff_N$	0.8	1.0	1.2	µm	100x1.2µm
Width Encroachment	ΔW_N		0.6		µm	Per side
Punch Through Voltage	$BVDSS_N$	9			V	
Poly Field Threshold Voltage	$VTF_{P(N)}$	10			V	

P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_P	–0.5	–0.7	–0.9	V	100x1.2µm
Body Factor	γ_P		0.45		$V^{1/2}$	100x1.2µm
Conduction Factor	β_P	24	28	32	$\mu A/V^2$	100x100µm
Effective Channel Length	$Leff_P$	0.9	1.1	1.3	µm	100x1.2µm
Width Encroachment	ΔW_P		0.8		µm	Per side
Punch Through Voltage	$BVDSS_P$	–9			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–10			V	

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Base Resistor Sheet Resist.	ρ_{RB}	1.30	1.60	2.00	KΩ/□	
Base Resistor Effective Width Change	ΔW_{RB}	–0.2	–0.6	–1.0	µm	
Base Resistor Voltage Coefficient, Narrow Size	$VOLTCO\_N$		11297		ppm/V	250x5µm
Base Resistor Voltage Coefficient, Wide Size	$VOLTCO\_W$		15468		ppm/V	250x25µm
Base Resistor Voltage Coefficient, Narrow Size	$TEMPCO\_N$		2761		ppm/C	250x5µm

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}	1.34	1.44	1.57	$fF/\mu m^2$	
Metal-1 to Poly-1	C_{M1P}		0.046		$fF/\mu m^2$	
Metal-1 to Silicon	C_{M1S}		0.046		$fF/\mu m^2$	
Metal-2 to Metal-1	C_{MM}		0.038		$fF/\mu m^2$	

Electrical Characteristics

NPN Bipolar Transistor Characteristics (Emitter size 4.5 x 4.5μm)

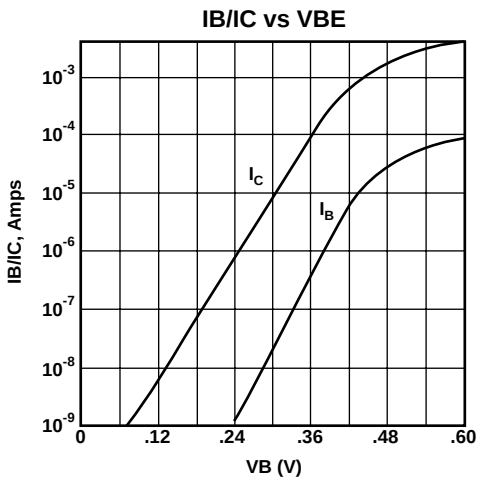
	Sym	Min	Typ	Max	Unit	Comments
Current Gain	h_{FE}		110			@100μA
Early Voltage	V_A		30		V	
Cut - Off Frequency	f_τ		6.2		GHz	
Collector-Emitter Saturation Voltage	V_{CESAT}		0.9		V	
Collector to Emitter Breakdown Voltage	BV_{CEO}		6.0		V	
Collector to Base Breakdown Voltage	BV_{CBO}		20		V	
Emitter to Base Breakdown Voltage	BV_{EBO}		7.0		V	
Emitter Resistance	R_E		30		Ω	
Base Spreading Resistance	R_B		1000		Ω	
Collector Saturation Resistance	R_C		450		Ω	
Base to Emitter Capacitance	C_{BEO}				pF	
Base to Collector Capacitance	C_{BCO}				pF	
Base to Substrate Capacitance	C_{CS}				pF	

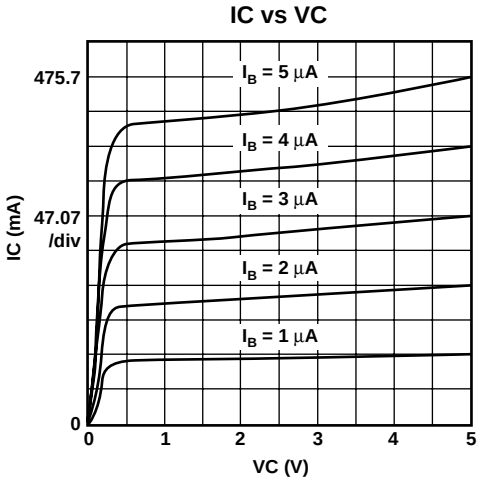
NPN Bipolar Transistor Characteristics (Emitter size 31.5 x 4.5μm)

	Sym	Min	Typ	Max	Unit	Comments
Current Gain	h_{FE}		100			@100μA
Early Voltage	V_A		30		V	
Cut - Off Frequency	f_τ		6.4		GHz	
Collector-Emitter Saturation Voltage	V_{CESAT}		0.45		V	
Collector to Emitter Breakdown Voltage	BV_{CEO}		6.0		V	
Collector to Base Breakdown Voltage	BV_{CBO}		20.0		V	
Emitter to Base Breakdown Voltage	BV_{EBO}		7.0		V	
Emitter Resistance	R_E		6		Ω	
Base Spreading Resistance	R_B		250		Ω	
Collector Saturation Resistance	R_C		65		Ω	

Physical Characteristics

Starting Material	p <100>	N+/P+ Width/Space	2.5/1.2µm
Starting Mat. Resistivity	25 - 50 Ω-cm	N+ to P+ Space	9.0µm
Typ. Operating Voltage	5V	Contact to Poly Space	1.5µm
Well Type	Twin well	Contact Overlap of Diffusion	1.0µm
Metal Layers	2	Contact Overlap of Poly	1.0µm
Poly Layers	1	Metal-1 Overlap of Contact	1.0µm
Contact Size	1.5x1.5µm	Metal-1 Overlap of Via	1.0µm
Via Size	1.5x1.5µm	Metal-2 Overlap of Via	1.0µm
Metal-1 Width/Space	2.5 / 1.5µm	Minimum Pad Opening	65x65µm
Metal-2 Width/space	2.5 / 1.5µm	Minimum Pad-to-Pad Spacing	5.0µm
Gate Poly Width/Space	1.5 / 2.0µm	Minimum Pad Pitch	80.0µm





Process C1226
CMOS 1.2µm
100V CMOS, Double Metal - Double Poly

Electrical Characteristics

T=25°C Unless otherwise noted

	Symbol	Minimum	Typical	Maximum	Unit	Comments
N-Channel High Voltage Transistor						
Threshold Voltage	HVT_N	0.70	0.90	1.10	V	
Punch Through Voltage	$HVBVDSS_N$	120			V	
ON Resistance	$HVPR_{0N}$	550	700	850	Ω	W/L = 147/5
Operating Voltage			V_{GS} = 5V V_{DS} = 100V			
N-Channel Low Voltage Transistor						
Threshold Voltage	VT_N	0.30	0.45	0.65	V	100x1.5µm
Body Factor	γ_N		0.475		$V^{1/2}$	100x1.5µm
Conduction Factor	β_N	64	78	92	µA/V²	100x100µm
Effective Channel Length	$Leff_N$		1.35		µm	100x1.5µm
Width Encroachment	ΔW_N		0.4		µm	Per side
Punch Through Voltage	$BVDSS_N$	5	12		V	
Poly Field Threshold Voltage	$VTFP_N$	8	15		V	

	Symbol	Minimum	Typical	Maximum	Unit	Comments
P-Channel High Voltage Transistor						
Threshold Voltage	HVT_P	–0.70	–0.90	–1.10	V	
Punch Through Voltage	$HVBVDSS_P$	–120			V	
ON Resistance	$HVPR_{0N}$	2000	2500	3000	Ω	W/L = 139/5
Operating Voltage			V_{GS}=5V V_{DS}=100V		V	
P-Channel Low Voltage Transistor						
Threshold Voltage	VT_P	-0.65	–0.45	–0.30	V	100x1.5µm
Body Factor	γ_P		0.6		$V^{1/2}$	100x1.5µm
Conduction Factor	β_P	20	25	30	µA/V²	100x100µm
Effective Channel Length	$Leff_P$		1.5		µm	100x1.5µm
Width Encroachment	ΔW_P		0.4		µm	Per side
Punch Through Voltage	$BVDSS_P$	–5	–12		V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–8	–12		V	

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}		TBD		fF/µm²	
Metal-1 to Poly1	C_{M1P}		TBD		fF/µm²	
Metal-2 to Metal-1	C_{MM}		TBD		fF/µm²	

Physical Characteristics

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Starting Material p<100>						
Well (field) Sheet Resistance	$\rho_{N\text{-}well(f)}$	1.0	1.7	2.4	KΩ/□	n-well
N+ Sheet Resistance	ρ_{N+}	20	35	50	Ω/□	
N+ Junction Depth	x_{jN+}		0.3		µm	
P+ Sheet Resistance	ρ_{P+}	60	110	150	Ω/□	
P+ Junction Depth	x_{jP+}		0.3		µm	
High-Voltage Gate Oxide Th	HT_{GOX}		24		nm	
Gate Oxide Thickness	T_{GOX}		24		nm	
Interpoly Oxide	IP_{OX}	33.6	42.0	50.4	nm	
Gate Poly Sheet Resistance	ρ_{POLY1}				Ω/□	
Metal-1 Sheet Resistance	ρ_{M1}				mΩ/□	
Metal-2 Sheet Resistance	ρ_{M2}				mΩ/□	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Layout Rules

High Voltage Section Rules

Min Channel Width	4.0µm	Contact Overlap of Diffusion	1.0µm
Min Spacing, Active Region, 5V	2.0µm	Contact Overlap of Poly	1.0µm
Poly1 Width/Space	1.5/2.0µm	Contact to Poly Space	1.5µm
Poly2 Width/Space	3.0/2.0µm	Metal-1 Overlap of Contact	1.0µm
Contact Width/Space	1.5/1.5µm	Minimum Pad Opening	65x65µm
Via Width/Space	1.5/1.5µm	Minimum Pad to Pad Spacing	5.0µm
Metal-1 Width/Space	2.5/1.5µm	Minimum Pad Pitch	80µm
Metal-2 Width/Space	2.5/1.5µm		

Process C1227
HV BiCMOS 1.2µm
30V Double Metal - Double Poly

Electrical Characteristics

T=25°C Unless otherwise noted

	Symbol	Minimum	Typical	Maximum	Unit	Comments
N-Channel High Voltage Transistor						
Threshold Voltage	HVT_N	0.7	0.9	1.1	V	
Punch Through Voltage	$HVBVDSS_P$	36			V	
ON Resistance	$HVPR_{0N}$		1.4		mΩ-cm²	@V_{GS} = 5V V_{DS} = 0.1V
Operating Voltage			V_{GS} = 5V V_{DS} = 30V		V	
N-Channel Low Voltage Transistor						
Threshold Voltage	VT_N	0.4	0.6	0.8	V	100x1.4µm
Body Factor	γ_N	0.50	0.65	0.80	$V^{1/2}$	100x1.4µm
Conduction Factor	β_N	64.0	75.0	86.0	µA/V²	100x100µm
Effective Channel Length	$Leff_N$	1.20	1.35	1.50	µm	100x1.4µm
Width Encroachment	ΔW_N		0.45		µm	Per side
Punch Through Voltage	$BVDSS_N$	8			V	
Poly Field Threshold Voltage	$VTFP_N$	10	18		V	

	Symbol	Minimum	Typical	Maximum	Unit	Comments
P-Channel High Voltage Transistor						
Threshold Voltage	HVT_P	–0.7	–0.9	–1.1	V	
Punch Through Voltage	$HVBVDSS_P$	–36			V	
ON Resistance	$HVPR_{0N}$		11.0		mΩ-cm²	@V_{GS} = –5V @V_{DS} = –0.1V
P-Channel Low Voltage Transistor						
Threshold Voltage	VT_P	–0.8	–0.6	–0.4	V	100x1.4µm
Body Factor	γ_P	0.35	0.50	0.65	$V^{1/2}$	100x1.4µm
Conduction Factor	β_P	20.0	25.0	30.0	µA/V²	100x100µm
Effective Channel Length	$Leff_P$	1.35	1.50	1.65	µm	100x1.4µm
Width Encroachment	ΔW_P		0.40		µm	Per side
Punch Through Voltage	$BVDSS_P$	–8			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–10	–18		V	

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}	1.338	1.439	1.569	fF/µm²	
Metal-1 to Poly1	C_{M1P}	0.040	0.046	0.052	fF/µm²	
Metal-2 to Metal-1	C_{MM}	0.043	0.050	0.057	fF/µm²	

Vertical NPN Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Beta	h_{FE}	50	140	240		4.5x4.5µm
Early Voltage	V_A		34		V	
Cut-Off Frequency	f_τ		1.89		GHz	

Physical Characteristics

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Starting Material p<100>						
Well(field)Sheet Resistance	$\rho_{N\text{-}well(f)}$	1.5	2.1	2.7	KΩ/□	n-well
N+ Sheet Resistance	ρ_{N+}	20.0	35.0	50.0	Ω/□	
N+ Junction Depth	x_{jN+}		0.4		μm	
P+ Sheet Resistance	ρ_{P+}	50.0	75.0	100.0	Ω/□	
P+ Junction Depth	x_{jP+}		0.4		μm	
Base Resistance	RSHB_RB	1.33	1.66	2.00	KΩ/sq	
High-Voltage Gate Oxide	HT_{GOX}		22		nm	
Gate Oxide Thickness	T_{GOX}		22		nm	
Interpoly Oxide Thickness	IP_{OX}	33.6	42	50.4	nm	
Gate Poly Sheet Resistance	ρ_{POLY1}	15.0	22.0	30.0	Ω/□	
Poly2 Resistivity	RSH_PL P	1.5	2	2.5	kΩ/□	
Metal-1 Sheet Resistance	ρ_{M1}	35.0	45.0	65.0	mΩ/□	
Metal-2 Sheet Resistance	ρ_{M2}	19.0	25.0	35.0	mΩ/□	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nitride

Layout Rules

Min Channel Width	4.0μm	Diffusion Overlap of Contact	1.0μm
Min Spacing, Active Region, 5V	2.0μm	Poly Overlap of Contact	1.0μm
Poly1 Width/Space	1.4/2.0μm	Metal-1 Overlap of Contact	1.5μm
Poly2 Width/Space	3.0/2.0μm	Contact to Poly Space	1.5μm
Contact Width/Space	1.4x1.4μm	Minimum Pad Opening	65x65μm
Via Width/Space	1.4/1.6μm	Metal-1 Overlap of Via	1.0μm
Metal-1 Width/Space	2.6/1.6μm	Metal-2 Overlap of Via	1.0μm
Metal-2 Width/Space	2.6/1.6μm	Minimum Pad Opening	65x65μm
Gate Poly Width/Space	1.5/2.0μm	Minimum Pad to Pad Spacing	5.0μm
N+/P+ Width/Space	2.5/2.0μm	Minimum Pad Pitch	80μm

Process C1229
HV CMOS 1.2μm
30V Double Metal - Double Poly

Electrical Characteristics

T=25°C Unless otherwise noted

	Symbol	Minimum	Typical	Maximum	Unit	Comments
N-Channel High Voltage Transistor						
Threshold Voltage	HVT_N	0.7	0.9	1.1	V	
Punch Through Voltage	$HVBVDSS_P$	36			V	
ON Resistance	$HVPR_{0N}$		1.4		mΩ-cm²	@V_{GS} = 5V V_{DS} = 0.1V
Operating Voltage			V_{GS} = 5V V_{DS} = 30V		V	
N-Channel Low Voltage Transistor						
Threshold Voltage	VT_N	0.4	0.6	0.8	V	100x1.4μm
Body Factor	γ_N	0.50	0.65	0.80	$V^{1/2}$	100x1.4μm
Conduction Factor	β_N	64.0	75.0	86.0	μA/V²	100x100μm
Effective Channel Length	$Leff_N$	1.20	1.35	1.50	μm	100x1.4μm
Width Encroachment	ΔW_N		0.45		μm	Per side
Punch Through Voltage	$BVDSS_N$	8			V	
Poly Field Threshold Voltage	$VTFP_N$	10	18		V	

	Symbol	Minimum	Typical	Maximum	Unit	Comments
P-Channel High Voltage Transistor						
Threshold Voltage	HVT_P	−0.7	−0.9	−1.1	V	
Punch Through Voltage	$HVBVDSS_P$	−36			V	
ON Resistance	$HVPR_{0N}$		11.0		mΩ-cm²	@V_{GS} = −5V @V_{DS} = −01V
P-Channel Low Voltage Transistor						
Threshold Voltage	VT_P	−0.8	−0.6	−0.4	V	100x1.4μm
Body Factor	γ_P	0.35	0.50	0.65	$V^{1/2}$	100x1.4μm
Conduction Factor	β_P	20.0	25.0	30.0	μA/V²	100x100μm
Effective Channel Length	$Leff_P$	1.35	1.50	1.65	μm	100x1.4μm
Width Encroachment	ΔW_P		0.40		μm	Per side
Punch Through Voltage	$BVDSS_P$	−8			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	−10	−18		V	

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}	1.338	1.439	1.569	fF/μm²	
Metal-1 to Poly1	C_{M1P}	0.040	0.046	0.052	fF/μm²	
Metal-2 to Metal-1	C_{MM}	0.043	0.050	0.057	fF/μm²	

Physical Characteristics

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Starting Material p<100>						
Well(field)Sheet Resistance	$\rho_{N\text{-}well(f)}$	1.5	2.1	2.7	KΩ/□	n-well
N+ Sheet Resistance	ρ_{N+}	20.0	35.0	50.0	Ω/□	
N+ Junction Depth	x_{jN+}		0.4		μm	
P+ Sheet Resistance	ρ_{P+}	50.0	75.0	100.0	Ω/□	
P+ Junction Depth	x_{jP+}		0.4		μm	
Base Resistance	RSHB_RB	1.33	1.66	2.00	KΩ/sq	
High-Voltage Gate Oxide	HT_{GOX}		22		nm	
Gate Oxide Thickness	T_{GOX}		22		nm	
Interpoly Oxide Thickness	IP_{OX}	33.6	42	50.4	nm	
Gate Poly Sheet Resistance	ρ_{POLY1}	15.0	22.0	30.0	Ω/□	
Poly2 Resistivity	RSH_PL P	1.5	2	2.5	kΩ/□	
Metal-1 Sheet Resistance	ρ_{M1}	35.0	45.0	65.0	mΩ/□	
Metal-2 Sheet Resistance	ρ_{M2}	19.0	25.0	35.0	mΩ/□	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nitride

Layout Rules

Min Channel Width	4.0μm	Diffusion Overlap of Contact	1.0μm
Min Spacing, Active Region, 5V	2.0μm	Poly Overlap of Contact	1.0μm
Poly1 Width/Space	1.4/2.0μm	Metal-1 Overlap of Contact	1.5μm
Poly2 Width/Space	3.0/2.0μm	Contact to Poly Space	1.5μm
Contact Width/Space	1.4x1.4μm	Minimum Pad Opening	65x65μm
Via Width/Space	1.4/1.6μm	Metal-1 Overlap of Via	1.0μm
Metal-1 Width/Space	2.6/1.6μm	Metal-2 Overlap of Via	1.0μm
Metal-2 Width/Space	2.6/1.6μm	Minimum Pad Opening	65x65μm
Gate Poly Width/Space	1.5/2.0μm	Minimum Pad to Pad Spacing	5.0μm
N+/P+ Width/Space	2.5/2.0μm	Minimum Pad Pitch	80μm

Process C1230

BiCMOS 1.2µm

Low TCR P-Poly for Analog

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_N	0.55	0.75	0.95	V	100x1.2µm
Body Factor	γ_N		0.34		$V^{1/2}$	100x1.2µm
Conduction Factor	β_N	64	75	86	$\mu A/V^2$	100x100µm
Effective Channel Length	$Leff_N$	0.8	1.0	1.2	µm	100x1.2µm
Width Encroachment	ΔW_N		0.6		µm	Per side
Punch Through Voltage	$BVDSS_N$	9			V	
Poly Field Threshold Voltage	$VTF_{P(N)}$	10			V	

P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_P	–0.7	–0.9	–1.1	V	100x1.2µm
Body Factor	γ_P		0.38		$V^{1/2}$	100x1.2µm
Conduction Factor	β_P	21	25	29	$\mu A/V^2$	100x100µm
Effective Channel Length	$Leff_P$	0.9	1.1	1.3	µm	100x1.2µm
Width Encroachment	ΔW_P		0.8		µm	Per side
Punch Through Voltage	$BVDSS_P$	–9			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–10			V	

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Base Resistor Sheet Resist.	ρ_{RB}	1.33	1.66	2.00	KΩ/□	
Base Resistor Effective Width Change	ΔW_{RB}	–0.2	–0.6	–1.0	µm	
Base Resistor Voltage Coefficient, Narrow Size	V_{OLTCO_N}		11297		ppm/V	250x5µm
Base Resistor Voltage Coefficient, Wide Size	V_{OLTCO_W}		15468		ppm/V	250x25µm
Base Resistor Voltage Coefficient, Narrow Size	T_{EMPCO_N}		2761		ppm/C	250x5µm
Low TCR P-Poly Resistor	$\rho_{HI\text{-}POLY}$	1.5	2.36	2.5	KΩ/□	
Temperature Coefficient - Low TCR Poly	TCR Poly	–100	0	+50	ppm/C	
Base to Emitter Capacitance	C_{BEO}		33.8		$fF/\mu m^2$	
Base to Collector Cap.	C_{BCO}		56.9		$fF/\mu m^2$	
Base to Substrate Cap.	C_{CS}		35.1		$fF/\mu m^2$	
Collector to Substrate Junction Capacitance	C_{JS}		0.1		$fF/\mu m^2$	

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}	1.28	1.38	1.58	$fF/\mu m^2$	
Metal-1 to Poly-1	C_{M1P}		0.057		$fF/\mu m^2$	
Metal-1 to Silicon	C_{M1S}		0.028		$fF/\mu m^2$	
Metal-2 to Metal-1	C_{MM}		0.035		$fF/\mu m^2$	
Poly-1 to Poly-2	C_{P1P2}	0.69	0.86	1.03	$fF/\mu m^2$	

Electrical Characteristics

NPN Bipolar Transistor Characteristics (Emitter size 4.5 x 4.5μm)

	Sym	Min	Typ	Max	Unit	Comments
Current Gain	h_{FE}		118			@100μA
Early Voltage	V_A		22		V	
Cut - Off Frequency	f_τ		6.2		GHz	
Collector-Emitter Saturation Voltage	V_{CESAT}		0.3		V	
Collector to Emitter Breakdown Voltage	BV_{CEO}		6.5		V	
Collector to Base Breakdown Voltage	BV_{CBO}		17		V	
Emitter to Base Breakdown Voltage	BV_{EBO}		6		V	
Emitter Resistance	R_E		40		Ω	
Base Spreading Resistance	R_B		1000		Ω	
Collector Saturation Resistance	R_C		100		Ω	
Base to Emitter Capacitance	C_{BEO}				pF	
Base to Collector Capacitance	C_{BCO}				pF	
Base to Substrate Capacitance	C_{CS}				pF	

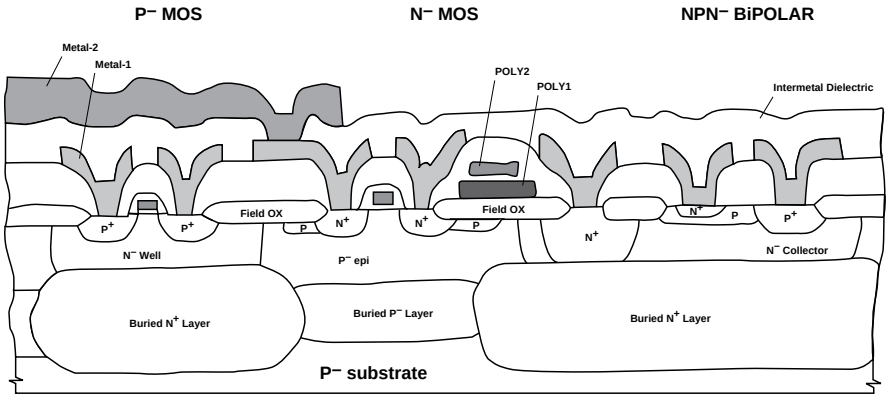
NPN Bipolar Transistor Characteristics (Emitter size 31.5 x 4.5μm)

	Sym	Min	Typ	Max	Unit	Comments
Current Gain	h_{FE}		110			@100μA
Early Voltage	V_A		22		V	
Cut - Off Frequency	f_τ		6.4		GHz	
Collector-Emitter Saturation Voltage	V_{CESAT}		0.2		V	
Collector to Emitter Breakdown Voltage	BV_{CEO}		6.5		V	
Collector to Base Breakdown Voltage	BV_{CBO}		17		V	
Emitter to Base Breakdown Voltage	BV_{EBO}		6		V	
Emitter Resistance	R_E		6		Ω	
Base Spreading Resistance	R_B		250		Ω	
Collector Saturation Resistance	R_C		15		Ω	

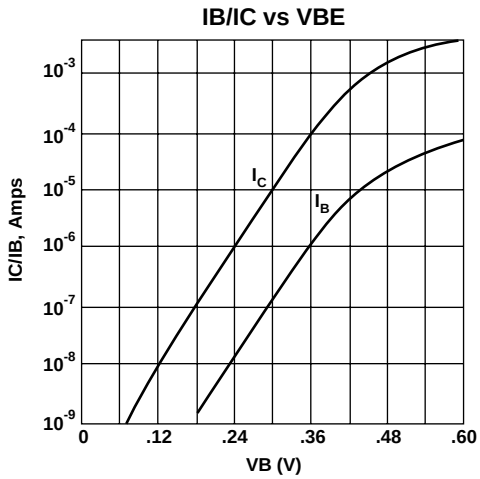
Physical Characteristics

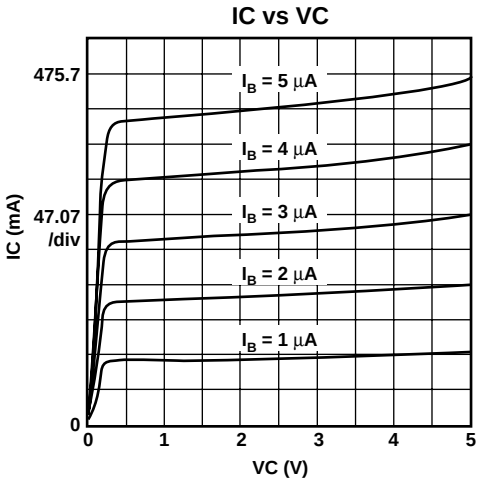
Starting Material	p <100>	N+/P+ Width/Space	2.5/1.2µm
Starting Mat. Resistivity	25 - 50 Ω-cm	N+ to P+ Space	9.0µm
Typ. Operating Voltage	5V	Contact to Poly Space	1.5µm
Well Type	N-well	Contact Overlap of Diffusion	1.0µm
Metal Layers	2	Contact Overlap of Poly	1.0µm
Poly Layers	2	Metal-1 Overlap of Contact	1.0µm
Contact Size	1.5x1.5µm	Metal-1 Overlap of Via	1.0µm
Via Size	1.5x1.5µm	Metal-2 Overlap of Via	1.0µm
Metal-1 Width/Space	2.5 / 1.5µm	Minimum Pad Opening	65x65µm
Metal-2 Width/space	2.5 / 1.5µm	Minimum Pad-to-Pad Spacing	5.0µm
Gate Poly Width/Space	1.5 / 2.0µm	Minimum Pad Pitch	80.0µm

Special feature of C1206 Process: BiCMOS 1.2-µm technology with a cutoff frequency of 6.4GHz.



Cross-sectional view of the BiCMOS 1.2 C1230 process





Process C1231
HV BiCMOS 1.2μm
30V Double Metal - Double Poly

Electrical Characteristics

T=25°C Unless otherwise noted

	Symbol	Minimum	Typical	Maximum	Unit	Comments
N-Channel High Voltage Transistor						
Threshold Voltage	HVT_N	0.45	0.65	0.85	V	
Punch Through Voltage	$HVBVDSS_P$	36			V	
ON Resistance	$HVPR_{0N}$		1.4		mΩ-cm²	@V_{GS} = 5V @V_{DS} = 0.1V
Operating Voltage			V_{GS} = 5V V_{DS} = 30V		V	
N-Channel Low Voltage Transistor						
Threshold Voltage	VT_N	0.6	0.8	1.00	V	100x1.4μm
Body Factor	γ_N	0.65	0.8	0.95	$V^{1/2}$	100x1.4μm
Conduction Factor	β_N	64.0	75.0	86.0	μA/V²	100x100μm
Effective Channel Length	$Leff_N$	1.20	1.35	1.50	μm	100x1.4μm
Width Encroachment	ΔW_N		0.45		μm	Per side
Punch Through Voltage	$BVDSS_N$	8			V	
Poly Field Threshold Voltage	$VTFP_N$	10	18		V	

	Symbol	Minimum	Typical	Maximum	Unit	Comments
P-Channel High Voltage Transistor						
Threshold Voltage	HVT_P	−0.7	−0.9	−1.1	V	
Punch Through Voltage	$HVBVDSS_P$	−36			V	
ON Resistance	$HVPR_{0N}$		11.0		mΩ-cm²	@V_{GS} = 5V
P-Channel Low Voltage Transistor						
Threshold Voltage	VT_P	−0.9	−0.7	−0.5	V	100x1.4μm
Body Factor	γ_P	0.25	0.40	0.55	$V^{1/2}$	100x1.4μm
Conduction Factor	β_P	20.0	25.0	30.0	μA/V²	100x100μm
Effective Channel Length	$Leff_P$	1.35	1.50	1.65	μm	100x1.4μm
Width Encroachment	ΔW_P		0.40		μm	Per side
Punch Through Voltage	$BVDSS_P$	−8			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	−10	−18		V	

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}	1.338	1.439	1.569	fF/μm²	
Metal-1 to Poly1	C_{M1P}	0.040	0.046	0.052	fF/μm²	
Metal-2 to Metal-1	C_{MM}	0.043	0.050	0.057	fF/μm²	

	Symbol	Minimum	Typical	Maximum	Unit	Comments
High Voltage Vertical NPN Transistor						
Beta	h_{FE}		130			
Early Voltage	V_A		200		V	
BV_{CEO}	BV_{CEO}		35		V	
Low Voltage Vertical NPN Transistor						
Beta	h_{FE}	50	140	240		4.5x4.5μm
Early Voltage	V_A		34		V	
Cut-Off Frequency	f_τ		1.89		GHz	

Physical Characteristics

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Starting Material p<100>						
Well(field)Sheet Resistance	$\rho_{N\text{-}well(f)}$	1.5	2.1	2.7	KΩ/□	n-well
N+ Sheet Resistance	ρ_{N+}	20.0	35.0	50.0	Ω/□	
N+ Junction Depth	x_{jN+}		0.4		μm	
P+ Sheet Resistance	ρ_{P+}	50.0	75.0	100.0	Ω/□	
P+ Junction Depth	x_{jP+}		0.4		μm	
Base Resistance	RSHB_RB	1.33	1.66	2.00	KΩ/sq	
High-Voltage Gate Oxide	HT_{GOX}		22		nm	
Gate Oxide Thickness	T_{GOX}		22		nm	
Interpoly Oxide Thickness	IP_{OX}	33.6	42	50.4	nm	
Gate Poly Sheet Resistance	ρ_{POLY1}	15.0	22.0	30.0	Ω/□	
Poly2 Resistivity	RSH_PL P	1.5	2	2.5	kΩ/□	
Metal-1 Sheet Resistance	ρ_{M1}	35.0	45.0	65.0	mΩ/□	
Metal-2 Sheet Resistance	ρ_{M2}	19.0	25.0	35.0	mΩ/□	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nitride

Layout Rules

Min Channel Width	4.0μm	Diffusion Overlap of Contact	1.0μm
Min Spacing, Active Region, 5V	2.0μm	Poly Overlap of Contact	1.0μm
Poly1 Width/Space	1.4/2.0μm	Metal-1 Overlap of Contact	1.5μm
Poly2 Width/Space	3.0/2.0μm	Contact to Poly Space	1.5μm
Contact Width/Space	1.4x1.4μm	Minimum Pad Opening	65x65μm
Via Width/Space	1.4/1.6μm	Metal-1 Overlap of Via	1.0μm
Metal-1 Width/Space	2.6/1.6μm	Metal-2 Overlap of Via	1.0μm
Metal-2 Width/Space	2.6/1.6μm	Minimum Pad Opening	65x65μm
Gate Poly Width/Space	1.5/2.0μm	Minimum Pad to Pad Spacing	5.0μm
N+/P+ Width/Space	2.5/2.0μm	Minimum Pad Pitch	80μm

Process C1232
CMOS 1.2µm
EEPROM with Lateral PNP

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_N	0.30	0.475	0.65	V	100x10µm
Body Factor	γ_N	0.35	0.45	0.55	$V^{1/2}$	100x100µm
Conduction Factor	β_N	64	78	92	$\mu A/V^2$	100x100µm
Saturation Current	I_{DSATN}	16	25	40	mA	100x1.5µm
Punch Through Voltage	$BVDSS_N$	5			V	
Poly Field Threshold	$VTF_{P(N)}$	8			V	

N-Channel Native Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_{ZBN}	–0.20	0.37	0.52	V	100x2.5µm
Body Factor	γ_{ZBN}	0.30	0.45	0.60	$V^{1/2}$	100x2.5µm
Saturation Current	I_{DSATN}	13	15.7	18.9	mA	100x2.5µm
Conduction Factor	β_{ZBN}	45	55	65	$\mu A/V^2$	100x100µm

P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_P	–0.65	–0.475	0.30	V	100x1.2µm
Body Factor	γ_P	0.5	0.6	0.7	$V^{1/2}$	100x1.2µm
Conduction Factor	β_P	20	25	30	$\mu A/V^2$	100x100µm
Saturation Current	I_{DSATP}	–6	–10	–16	mA	100x1.5µm
Punch Through Voltage	$BVDSS_P$	–5			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–8			V	

EECMOS Characteristics	Symbol	Minimum	Typical	Maximum	Unit	Comments
Tunnel Oxide Thickness	T_{TUNLOX}	84	88	92	nm	
Interpoly Oxide Thickness	T_{P1P2}	340	390	440	nm	
Buried N+ Sheet Res.	ρ_{BN+}	200	300	400	Ω/□	
Initial Program/Erase Window			3.0		V	
Unprog. Memory Threshold	V_T		3.0		V	
Endurance		10,000			Cycles	
Programming Voltage	VPP	12	14	17	V	

Lateral PNP	Symbol	Minimum	Typical	Maximum	Unit	Comments
Beta	H_{FE}	10	35	100		
Early Voltage	V_{AP}		TBD		V	

Electrical Characteristics

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{N\text{-well(f)}}$	1.2	20	2.8	KΩ/□	n-well
N+ Sheet Resistance	ρ_{N+}	20	35	50	Ω/□	
N+ Junction Depth	x_{jN+}		0.35		µm	
P+ Sheet Resistance	ρ_{P+}	60	110	160	Ω/□	
P+ Junction Depth	x_{jP+}		0.35		µm	
Gate Oxide Thickness	T_{GOX}	22.5	25.0	27.5	nm	
Field Oxide Thickness	T_{FIELD}		700		nm	
Gate Poly Sheet Res.	ρ_{POLY2}	25	35	45	Ω/□	
Bottom Poly Sheet Res.	ρ_{POLY1}	24	32	40	Ω/□	
High Resistance Poly	ρ_{POLYHI}	1.5	2.0	2.5	kΩ/□	
Metal-1 Sheet Resistance	ρ_{M1}		50		mΩ/□	
Metal-2 Sheet Resistance	ρ_{M2}	19	25	32	mΩ/□	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}	1.28	1.38	1.58	fF/µm²	
Metal-1 to Poly1	C_{M1P}		0.057		fF/µm²	
Metal-1 to Silicon	C_{M1S}		0.028		fF/µm²	
Metal-2 to Metal-1	C_{MM}		0.035		fF/µm²	
Poly-1 to Poly-2	C_{P1P1}		0.86		fF/µm²	

Physical Characteristics

Starting Material	P <100>	High Poly Width/Space	1.5 / 1.5µm
Starting Mat. Resistivity	25 - 50 Ω-cm	N+/P+ Width/Space	2.0 / 2.0µm
Epi Layer	P Type, 7 - 8.5 Ω-cm with N+ Buried Layer	N+ To P+ Space	9.0µm
		Tunnel Oxide Width/Space	1.5 / 1.5µm
Operating Voltage	5V	Tunnel Ox. Overlap Bot. Poly	1.0µm
Well Type	N-well	Contact To Poly Space	1.5µm
Metal Layers	2	Contact Overlap Of Diffusion	1.0µm
Poly Layers	2	Contact Overlap Of Poly	1.0µm
Contact Size	1.5x1.5µm	Metal-1 Overlap Of Contact	1.0µm
Via Size	1.5x1.5µm	Metal-1 Overlap Of Via	1.0µm
Metal-1 Width/Space	2.5 / 1.5µm	Metal-2 Overlap Of Via	1.0µm
Metal-2 Width/Space	2.5 / 1.5µm	Minimum Pad Opening	65x65µm
Gate Poly Width/Space	1.5 / 2.0µm	Minimum Pad-to-Pad Spacing	5.0µm
Buried N+ Width/Space	2.5 / 1.75µm	Minimum Pad Pitch	80.0µm

Special Feature of C1232 Process: EEPROM process with high resistivity poly resistors and native n-channel devices.

Process C1601
CMOS 1.6µm
Analog Mixed Mode

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_N	0.47	0.67	0.87	V	25x1.6µm
Body Factor	γ_N	0.6	0.75	0.90	$V^{1/2}$	25x1.6 µm
Conduction Factor	β_N	33	39	45	$\mu A/V^2$	25x25µm
Effective Channel Length	$Leff_N$	1.0	1.3	1.6	µm	25x1.6 µm
Width Encroachment	ΔW_N		0.0		µm	Per side
Punch Through Voltage	$BVDSS_N$	8			V	
Poly Field Threshold Voltage	$VTF_{P(N)}$	8			V	

P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_P	–1.1	–0.9	–0.7	V	25x1.6 µm
Body Factor	γ_P	0.27	0.42	0.57	$V^{1/2}$	25x1.6 µm
Conduction Factor	β_P	10.0	12.5	15.0	$\mu A/V^2$	25x25µm
Effective Channel Length	$Leff_P$	1.12	1.42	1.72	µm	25x1.6 µm
Width Encroachment	ΔW_P		0.0		µm	Per side
Punch Through Voltage	$BVDSS_P$	–8			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–8			V	

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{N\text{-well(f)}}$	1.6	2.0	2.4	KΩ/□	n-well
N+ Sheet Resistance	ρ_{N+}	25	35	45	Ω/□	
N+ Junction Depth	x_{jN+}		0.35		µm	
P+ Sheet Resistance	ρ_{P+}	74	94	114	Ω/□	
P+ Junction Depth	x_{jP+}		0.35		µm	
Gate Oxide Thickness	T_{GOX}	225	250	275	nm	
Field Oxide Thickness	T_{FIELD}	550	650	750	nm	
Gate Poly Sheet Resistance	ρ_{POLY1}	15	22	30	Ω/□	
Bottom Poly Sheet Res.	ρ_{POLY2}	29	37	45	Ω/□	
Metal-1 Sheet Resistance	ρ_{M1}		50		mΩ/□	
Metal-2 Sheet Resistance	ρ_{M2}		30		mΩ/□	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}	1.23	1.38	1.53	$fF/\mu m^2$	
Metal-1 to Poly-1	C_{M1P}		0.046		$fF/\mu m^2$	
Metal-2 to Metal-1	C_{MM}	0.033	0.037	0.041	$fF/\mu m^2$	
Metal-1 to Silicon	C_{M1S}	0.026	0.030	0.034	$fF/\mu m^2$	
Poly-1 to Poly-2	C_{P1P2}	0.43	0.53	0.63	$fF/\mu m^2$	

Physical Characteristics

Starting Material	P <100>	N+/P+ Width/Space	1.6 / 3.2µm
Starting Mat. Resistivity	15 - 25 Ω-cm	N+ To P+ Space	8.0µm
Typ. Operating Voltage	5V	Contact To Poly Space	1.5µm
Well Type	N-well	Contact Overlap Of Diffusion	0.8µm
Metal Layers	2	Contact Overlap Of Poly	0.8µm
Poly Layers	2	Metal-1 Overlap Of Contact	1.0µm
Contact Size	1.5x1.5µm	Metal-1 Overlap Of Via	1.0µm
Via Size	1.5x1.5µm	Metal-2 Overlap Of Via	1.2µm
Metal-1 Width/Space	2.0 / 2.0µm	Minimum Pad Opening	65x65µm
Metal-2 Width/Space	3.2 / 2.3µm	Minimum Pad-to-Pad Spacing	5.0µm
Gate Poly Width/Space	1.6 / 1.7µm	Minimum Pad Pitch	80.0µm

Special Feature of C1601 Process: 2.0 µm Analog process with n- and p-channel transistors in CMOS 1.5 µm technology.

Process C3013
CMOS 3μm
10 Volt Single Metal Analog

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_N	0.6	0.8	1.0	V	100x4μm
Body Factor	γ_N		0.6		$V^{1/2}$	100x4μm
Conduction Factor	β_N	42	47	52	$\mu A/V^2$	100x100μm
Effective Channel Length	$Leff_N$	2.85	3.2	3.55	μm	100x4μm
Width Encroachment	ΔW_N		0.7		μm	Per side
Punch Through Voltage	$BVDSS_N$	12			V	
Poly Field Threshold Voltage	$VTF_{P(N)}$	12			V	

P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_P	–0.6	–0.8	–1.0	V	100x4μm
Body Factor	γ_P		0.55		$V^{1/2}$	100x4μm
Conduction Factor	β_P	13	15	19	$\mu A/V^2$	100x100μm
Effective Channel Length	$Leff_P$	2.85	3.2	3.55	μm	100x4μm
Width Encroachment	ΔW_P		0.9		μm	Per side
Punch Through Voltage	$BVDSS_P$	–12			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–12			V	

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{P\text{-well(f)}}$	3.2	4.8	6.5	KΩ/□	P-well
N+ Sheet Resistance	ρ_{N+}	16	21	27	Ω/□	
N+ Junction Depth	x_{jN+}		0.8		μm	
P+ Sheet Resistance	ρ_{P+}	50	80	100	Ω/□	
P+ Junction Depth	x_{jP+}		0.7		μm	
Gate Oxide Thickness	T_{GOX}	44	48	52	nm	
Interpoly Oxide Thickness	T_{P1P2}		60		nm	
Gate Poly Sheet Resistance	ρ_{POLY1}	15	22	30	Ω/□	
Bottom Poly Sheet Res.	ρ_{POLY2}	15	22	30	Ω/□	
Metal-1 Sheet Resistance	ρ_{M1}		30	60	mΩ/□	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}	0.66	0.72	0.78	$fF/\mu m^2$	
Metal-1 to Poly-1	C_{M1P}		0.0523		$fF/\mu m^2$	
Metal-1 to Silicon	C_{M1S}	0.026	0.030	0.034	$fF/\mu m^2$	
Poly-1 to Poly-2	C_{P1P2}	0.51	0.57	0.63	$fF/\mu m^2$	

Physical Characteristics

Starting Material	N <100>	N+/P+ Width/Space	3.0 / 3.0µm
Starting Mat. Resistivity	15 - 25 Ω-cm	N+ To P+ Space	12µm
Typ. Operating Voltage	5V	Contact To Poly Space	2.5µm
Well Type	P-well	Contact Overlap Of Diffusion	1.5µm
Metal Layers	1	Contact Overlap Of Poly	1.0µm
Poly Layers	2	Metal-1 Overlap Of Contact	1.0µm
Contact Size	2.0x2.0µm	Minimum Pad Opening	100x100µm
Metal-1 Width/Space	3.5 / 2.5µm	Minimum Pad-to-Pad Spacing	55µm
Gate Poly Width/Space	4.0 / 2.5µm	Minimum Pad Pitch	80.0µm

Special Feature of C3013 Process: P-well analog process with single metal CMOS 3.0 µm technology for 10 Volt applications.

Process C3014
CMOS 3µm
5 Volt Single Metal Analog

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_N	0.5	0.65	0.8	V	100x3µm
Body Factor	γ_N		0.6		$V^{1/2}$	100x3µm
Conduction Factor	β_N	42	47	52	$\mu A/V^2$	100x100µm
Effective Channel Length	$Leff_N$	2.0	2.3	2.6	µm	100x3µm
Width Encroachment	ΔW_N		0.7		µm	Per side
Punch Through Voltage	$BVDSS_N$	12			V	
Poly Field Threshold Voltage	$VTF_{P(N)}$	12			V	

P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_P	–0.5	0.65	–0.8	V	100x3µm
Body Factor	γ_P		0.55		$V^{1/2}$	100x3µm
Conduction Factor	β_P	13	15	19	$\mu A/V^2$	100x100µm
Effective Channel Length	$Leff_P$	2.85	3.2	3.55	µm	100x3µm
Width Encroachment	ΔW_P		0.9		µm	Per side
Punch Through Voltage	$BVDSS_P$	–12			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–12			V	

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{P\text{-well(f)}}$	3.2	4.8	6.5	KΩ/□	P-well
N+ Sheet Resistance	ρ_{N+}	16	21	27	Ω/□	
N+ Junction Depth	x_{jN+}		0.8		µm	
P+ Sheet Resistance	ρ_{P+}	50	80	100	Ω/□	
P+ Junction Depth	x_{jP+}		0.7		µm	
Gate Oxide Thickness	T_{GOX}	44	48	52	nm	
Interpoly Oxide Thickness	T_{P1P2}		60		nm	
Gate Poly Sheet Resistance	ρ_{POLY1}	15	22	30	Ω/□	
Bottom Poly Sheet Res.	ρ_{POLY2}	20	30	40	Ω/□	
Metal-1 Sheet Resistance	ρ_{M1}		30	60	mΩ/□	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}	0.66	0.72	0.78	$fF/\mu m^2$	
Metal-1 to Poly-1	C_{M1P}		0.0523		$fF/\mu m^2$	
Metal-1 to Silicon	C_{M1S}	0.026	0.030	0.034	$fF/\mu m^2$	
Poly-1 to Poly-2	C_{P1P2}	0.51	0.57	0.63	$fF/\mu m^2$	

Physical Characteristics

Starting Material	N <100>	N+/P+ Width/Space	3.0 / 3.0µm
Starting Mat. Resistivity	15 - 25 Ω-cm	N+ To P+ Space	12µm
Typ. Operating Voltage	5V	Contact To Poly Space	2.5µm
Well Type	P-well	Contact Overlap Of Diffusion	1.5µm
Metal Layers	1	Contact Overlap Of Poly	1.0µm
Poly Layers	2	Metal-1 Overlap Of Contact	1.0µm
Contact Size	2.0x2.0µm	Minimum Pad Opening	100x100µm
Metal-1 Width/Space	3.5 / 2.5µm	Minimum Pad-to-Pad Spacing	55µm
Gate Poly Width/Space	4.0 / 2.5µm	Minimum Pad Pitch	80.0µm

Special Feature of C3014 Process: P-well analog low threshold process with single metal CMOS 3.0µm technology for 5 Volt applications.

Process C3015
CMOS 3μm Digital

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_N	0.6	0.8	1.0	V	100x3μm
Body Factor	γ_N		0.6		$V^{1/2}$	100x3μm
Conduction Factor	β_N	42	47	52	$\mu A/V^2$	100x100μm
Effective Channel Length	$Leff_N$	2.85	3.2	3.55	μm	100x3μm
Width Encroachment	ΔW_N		0.7		μm	Per side
Punch Through Voltage	$BVDSS_N$	12			V	
Poly Field Threshold Voltage	$VTF_{P(N)}$	12			V	

P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_P	–0.6	–0.8	–1.0	V	100x3μm
Body Factor	γ_P		0.55		$V^{1/2}$	100x3μm
Conduction Factor	β_P	13	15	19	$\mu A/V^2$	100x100μm
Effective Channel Length	$Leff_P$	2.85	3.2	3.55	μm	100x3μm
Width Encroachment	ΔW_P		0.9		μm	Per side
Punch Through Voltage	$BVDSS_P$	–12			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–12			V	

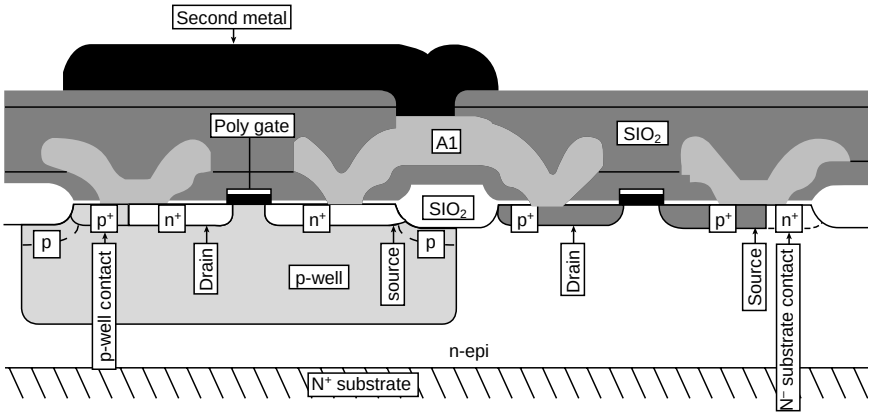
Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{P\text{-well(f)}}$	3.2	4.8	6.5	KΩ/□	P-well
N+ Sheet Resistance	ρ_{N+}	16	21	27	Ω/□	
N+ Junction Depth	x_{jN+}		0.8		μm	
P+ Sheet Resistance	ρ_{P+}	50	80	100	Ω/□	
P+ Junction Depth	x_{jP+}		0.7		μm	
Gate Oxide Thickness	T_{GOX}	37.5	40.0	42.5	nm	
Gate Poly Sheet Resistance	ρ_{POLY1}	15	22	30	Ω/□	
Metal-1 Sheet Resistance	ρ_{M1}		30	60	mΩ/□	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}	0.66	0.72	0.78	$fF/\mu m^2$	
Metal-1 to Poly-1	C_{M1P}		0.0523		$fF/\mu m^2$	
Metal-1 to Silicon	C_{M1S}	0.026	0.030	0.034	$fF/\mu m^2$	

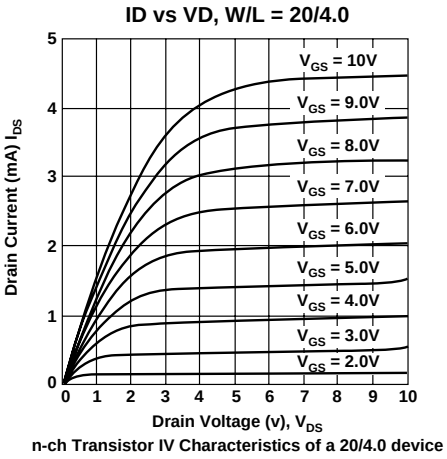
Physical Characteristics

Starting Material	N <100>	N+/P+ Width/Space	3.0 / 3.0µm
Starting Mat. Resistivity	15 - 25 Ω-cm	N+ To P+ Space	12µm
Typ. Operating Voltage	5V	Contact To Poly Space	2.5µm
Well Type	P-well	Contact Overlap Of Diffusion	1.5µm
Metal Layers	1	Contact Overlap Of Poly	1.0µm
Poly Layers	1	Metal-1 Overlap Of Contact	1.0 µm
Contact Size	2.0x2.0µm	Minimum Pad Opening	100x100µm
Metal-1 Width/Space	3.5 / 2.5µm	Minimum Pad-to-Pad Spacing	5.0µm
Gate Poly Width/Space	3.0 / 2.5µm	Minimum Pad Pitch	80.0µm

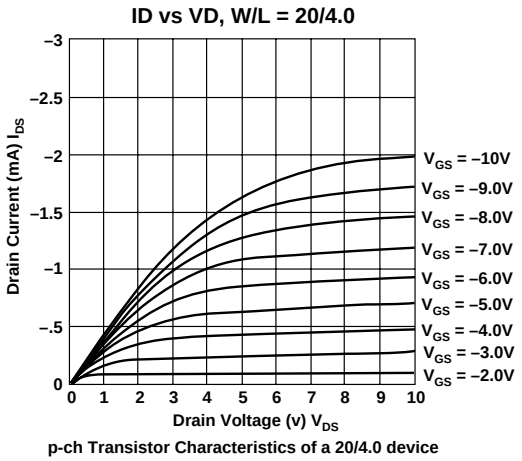
Special Feature of C3015 Process: 3 µm P-well digital process.



Cross-sectional view of the C3015 process



n-ch Transistor IV Characteristics of a 20/4.0 device



p-ch Transistor Characteristics of a 20/4.0 device

Process C3017
CMOS 3μm
10 Volt Analog Mixed Mode

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_N	0.6	0.8	1.0	V	100x4μm
Body Factor	γ_N		0.6		$V^{1/2}$	100x4μm
Conduction Factor	β_N	42	47	52	$\mu A/V^2$	100x100μm
Effective Channel Length	$Leff_N$	2.85	3.2	3.55	μm	100x4μm
Width Encroachment	ΔW_N		0.7		μm	Per side
Punch Through Voltage	$BVDSS_N$	12			V	
Poly Field Threshold Voltage	$VTF_{P(N)}$	12			V	

P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_P	–0.6	–0.8	–1.0	V	100x4μm
Body Factor	γ_P		0.55		$V^{1/2}$	100x4μm
Conduction Factor	β_P	13	15	19	$\mu A/V^2$	100x100μm
Effective Channel Length	$Leff_P$	2.85	3.2	3.55	μm	100x4μm
Width Encroachment	ΔW_P		0.9		μm	Per side
Punch Through Voltage	$BVDSS_P$	–12			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–12			V	

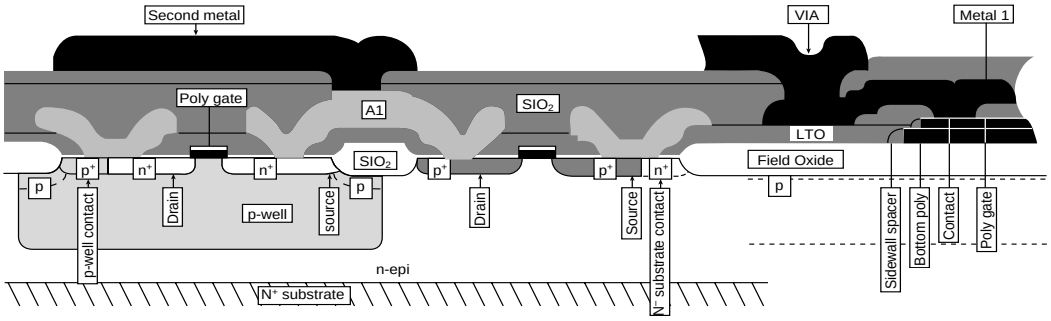
Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{P\text{-well(f)}}$	3.2	4.8	6.5	KΩ/□	P-well
N+ Sheet Resistance	ρ_{N+}	16	21	27	Ω/□	
N+ Junction Depth	x_{jN+}		0.8		μm	
P+ Sheet Resistance	ρ_{P+}	50	80	100	Ω/□	
P+ Junction Depth	x_{jP+}		0.7		μm	
Gate Oxide Thickness	T_{GOX}	44	48	52	nm	
Interpoly Oxide Thickness	T_{P1P2}		60		nm	
Gate Poly Sheet Resistance	ρ_{POLY1}	15	22	30	Ω/□	
Bottom Poly Sheet Res.	ρ_{POLY2}	15	22	30	Ω/□	
Metal-1 Sheet Resistance	ρ_{M1}		50		mΩ/□	
Metal-2 Sheet Resistance	ρ_{M2}		30		mΩ/□	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}	0.66	0.72	0.78	$fF/\mu m^2$	
Metal-1 to Poly-1	C_{M1P}		0.0523		$fF/\mu m^2$	
Metal-1 to Silicon	C_{M1S}	0.26	0.30	0.34	$fF/\mu m^2$	
Metal-2 to Metal-1	C_{MM}	0.033	0.0384	0.041	$fF/\mu m^2$	
Poly-1 to Poly-2	C_{P1P2}	0.51	0.57	0.63	$fF/\mu m^2$	

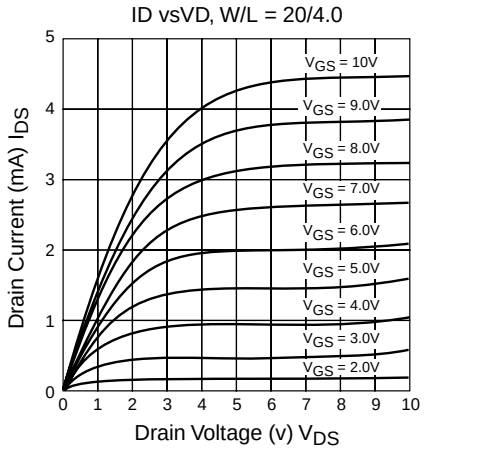
Physical Characteristics

Starting Material	P <100>	N+/P+ Width/Space	3.0 / 3.0µm
Starting Mat. Resistivity	15 - 25 Ω-cm	N+ To P+ Space	12µm
Typ. Operating Voltage	10V	Contact To Poly Space	2.5µm
Well Type	P-well	Contact Overlap Of Diffusion	1.5µm
Metal Layers	2	Contact Overlap Of Poly	1.0µm
Poly Layers	2	Metal-1 Overlap Of Contact	1.0µm
Contact Size	2.0x2.0µm	Metal-1 Overlap Of Via	1.75µm
Via Size	2.0x2.0µm	Metal-2 Overlap Of Via	1.5µm
Metal-1 Width/Space	3.5 / 2.5µm	Minimum Pad Opening	100x100µm
Metal-2 Width/Space	5.0 / 3.0µm	Minimum Pad-to-Pad Spacing	5.0µm
Gate Poly Width/Space	4.0 / 2.5µm	Minimum Pad Pitch	80.0 µm

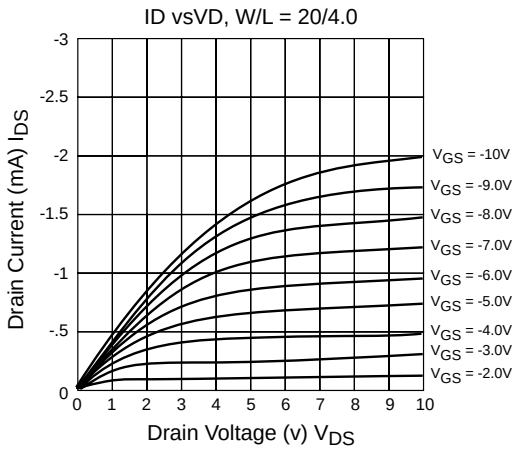
Special Feature of C3017 Process: P-well analog process with double metal CMOS 3.0 µm technology.



Cross-sectional view of the C3017 process



n-ch Transistor IV characteristics of a 20/4.0 device



p-ch Transistor IV characteristics of a 20/4.0 device

Process C3025
CMOS 3μm
10 Volt Analog

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_N	0.65	0.85	1.05	V	100x4μm
Body Factor	γ_N		0.87		$V^{1/2}$	100x4μm
Conduction Factor	β_N	40	48	56	$\mu A/V^2$	100x100μm
Effective Channel Length	$Leff_N$	3.05	3.40	3.75	μm	100x4μm
Width Encroachment	ΔW_N		0.550		μm	Per side
Punch Through Voltage	$BVDSS_N$	16.5			V	
Poly Field Threshold Voltage	$VTF_{P(N)}$	12			V	

P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_P	–0.7	–0.9	–1.1	V	100x4μm
Body Factor	γ_P		0.75		$V^{1/2}$	100x4μm
Conduction Factor	β_P	13	16	19	$\mu A/V^2$	100x100μm
Effective Channel Length	$Leff_P$	3.00	3.35	3.70	μm	100x4μm
Width Encroachment	ΔW_P		0.8		μm	Per side
Punch Through Voltage	$BVDSS_P$	–16.5			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–12			V	

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{P\text{-well(f)}}$	3.25	5.25	7.25	KΩ/□	P-well
N+ Sheet Resistance	ρ_{N+}	13	20	27	Ω/□	
N+ Junction Depth	x_{jN+}		0.8		μm	
P+ Sheet Resistance	ρ_{P+}	50	80	100	Ω/□	
P+ Junction Depth	x_{jP+}		0.7		μm	
Gate Oxide Thickness	T_{GOX}	45	48	51	nm	
Interpoly Oxide Thickness	T_{P1P2}	56	66	76	nm	
Gate Poly Sheet Resistance	ρ_{POLY1}	15	22	30	Ω/□	
Bottom Poly Sheet Res.	ρ_{POLY2}	15	22	30	Ω/□	
Metal-1 Sheet Resistance	ρ_{M1}		50		mΩ/□	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}	0.68	0.72	0.78	$fF/\mu m^2$	
Metal-1 to Poly-1	C_{M1P}	0.047	0.0523	0.0575	$fF/\mu m^2$	
Metal-1 to Silicon	C_{M1S}	0.027	0.30	0.034	$fF/\mu m^2$	
Poly-1 to Poly-2	C_{P1P2}	0.453	0.523	0.617	$fF/\mu m^2$	

Physical Characteristics

Starting Material	P <100>	N+/P+ Width/Space	3.0 / 3.0µm
Starting Mat. Resistivity	15 - 25 Ω-cm	N+ To P+ Space	12µm
Typ. Operating Voltage	10V	Contact To Poly Space	2.5µm
Well Type	P-well	Contact Overlap Of Active	1.5µm
Metal Layers	1	Contact Overlap Of Poly	1.0µm
Poly Layers	2	Metal-1 Overlap Of Contact	1.0µm
Contact Size	2.0x2.0µm	Minimum Pad Opening	100x100µm
Metal-1 Width/Space	3.5 / 2.5µm	Minimum Pad-to-Pad Spacing	5.0µm
Gate Poly Width/Space	3.0 / 3µm	Minimum Pad Pitch	80.0µm

Special Feature of C3025 Process: 10 Volt P-well single metal analog process.

Process C5014
CMOS 5μm
15 Volt Analog

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_N	0.7	0.9	1.0	V	100x100μm
Body Factor	γ_N	1.2	1.4	1.6	$V^{1/2}$	100x100μm
Conduction Factor	β_N	23	25.5	30	$\mu A/V^2$	100x100μm
Effective Channel Length	$Leff_N$	2.33	2.85	3.33	μm	100x100μm
Width Encroachment	ΔW_N		1.0		μm	Per side
Punch Through Voltage	$BVDSS_N$	20	25		V	
Poly Field Threshold Voltage	$VTF_{P(N)}$	20			V	

P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_P	-0.7	-0.9	-1.1	V	100x100μm
Body Factor	γ_P	0.6	0.75	0.9	$V^{1/2}$	100x100μm
Conduction Factor	β_P	7.5	9.0	10.5	$\mu A/V^2$	100x100μm
Effective Channel Length	$Leff_P$	2.92	3.34	3.82	μm	100x100μm
Width Encroachment	ΔW_P		1.5		μm	Per side
Punch Through Voltage	$BVDSS_P$	-20	-25		V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	-20			V	

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{P\text{-well(f)}}$	4	5	6	KΩ/□	P-well
N+ Sheet Resistance	ρ_{N+}	10	13	15	Ω/□	
N+ Junction Depth	x_{jN+}		1.5		μm	
P+ Sheet Resistance	ρ_{P+}	30	50	75	Ω/□	
P+ Junction Depth	x_{jP+}		1.2		μm	
Gate Oxide Thickness	T_{GOX}	100	108	118	nm	
Interpoly Oxide Thickness	T_{P1P2}	56	66	76	nm	
Gate Poly Sheet Resistance	ρ_{POLY1}	12	15	30	Ω/□	
Top Poly Sheet Res.	ρ_{POLY2}	20	30	40	Ω/□	
Metal-1 Sheet Resistance	ρ_{M1}		25	60	mΩ/□	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}		0.321		$fF/\mu m^2$	
Metal-1 to Poly-1	C_{M1P}		0.036		$fF/\mu m^2$	
Metal-1 to Silicon	C_{M1S}		0.019		$fF/\mu m^2$	
Poly-1 to Poly-2	C_{P1P2}	0.436	0.57	0.704	$fF/\mu m^2$	

Physical Characteristics

Starting Material	N <100>	N+/P+ Width/Space	3.0 / 5.0µm
Starting Mat. Resistivity	3 - 6 Ω-cm	N+ To P+ Space	5.0µm
Typ. Operating Voltage	15V	Contact To Poly Space	3.0µm
Well Type	P-well	Contact Overlap Of Active	2.0µm
Metal Layers	1	Contact Overlap Of Poly	1.0µm
Poly Layers	2	Metal-1 Overlap Of Contact	1.0µm
Contact Size	3.0x3.0µm	Minimum Pad Opening	100x100µm
Metal-1 Width/Space	5.0 / 3.0 µm	Minimum Pad-to-Pad Spacing	5.0µm
Gate Poly Width/Space	5.0 / 2.5µm	Minimum Pad Pitch	80.0µm

Special Feature of C5014 Process: 15 Volt P-well single metal analog process in CMOS 5.0 µm technology.

Test and Packaging Capability

Test and Packaging Capability

Test Equipment Capability

Manufacturer	Pins	Speed
Sentry 21	120	20MHz
Sentry 21	60	20MHz
Sentry 20	60	20MHz
LTX 77	24	10MHz Analog
LTX Synchro	48 Digital, 48 Analog	40MHz*
MCT	128	40MHz*

*MUX Capable to 80MHz

test&packaging_01.eps

Key Packaging Offering

Package Type	Lead Count
Plastic / Ceramic Dip	8, 14, 16. 18, 20, 24, 28, 40, 48
Plastic / Ceramic Chip Carrier	20, 28, 32, 44, 52, 68, 84
Plastic SOIC	8, 14, 16, 20, 24, 28, 32, 36, 48
Plastic SOJ	20/26, 48, 56
Plastic SSOP	20, 24, 28, 48, 56
Plastic QFP	44, 52, 64, 80, 100, 120, 128, 144, 160, 184, 208
Plastic TQFP	32, 48, 64, 80, 100, 144, 176
SOT	3, 4, 5, 6
Others	Consult Factory

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Assembly Vendors

Vendor	Location	Packages
AMT	Indonesia	DIP, PLCC, SOIC, QFP, TQFP
ASE	Malaysia, Taiwan	DIP, PLCC, SOIC, QFT, TQFP, SOJ, SSOP
Carsem	Malaysia	SSOP, QSOT, TSSOP, PQFP,TQFP
IPAC	U.S.	Plastic, QuickTurn Service
IN-HOUSE	U.S.	Ceramic Prototype

test&packaging_03.eps

ISO 9001 Registered

Quality at IMP - Our Policy

ISO 9001 Registered

Quality at IMP - Our Policy

Quality Priority

Quality in everything we do is a fundamental IMP commitment. Quality may not be sacrificed for any other priority. Before any action is taken, the effect on quality as seen by employees and by customers must be considered.

Product Quality Conformance

Products and services for our customers will conform to all requirements. Products will meet performance specifications. Services will be complete, meet described requirements, and will be in a format appropriate for the customer's use. If a specification cannot be met in full, the customer will be advised and a new specification will be negotiated.

Product and Process Quality Improvement

All processes, manufacturing, manufacturing planning, customer service, product design and design of manufacturing processes shall utilize Total Quality Management concepts including Statistical Process Control techniques and designed experiments to ensure continual improvement of products and services.

Employee Responsibility

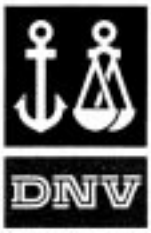
Each employee is responsible for performing their work correctly and completely. This responsibility for quality performance applies to all design work, development work, manufacturing work and to all supporting work. It applies to all employee levels. It cannot be abandoned or delegated. No one else can take responsibility.

IMP's Commitment of Support

IMP will provide the tools, the training, and the time necessary for employees to meet their responsibilities.

Employee Participation

IMP encourages all employees to take part in the open discussion, analysis and resolution of problems through participation in quality and productivity teams or through personal suggestions.



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of

IMP INC.

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Has been found to conform to Quality Standard:

ISO 9001, 1994

This Certificate is valid for the following products/service ranges:

DESIGN AND MANUFACTURE OF ANALOG AND MIXED-SIGNAL INTEGRATED CIRCUITS AND WAFER FABRICATION SERVICES

Place and date:

Houston, Texas; 01 November 1996

for the Accredited Unit:
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Management Representative
DNV Certification, Inc.

Accredited by
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This certificate is valid until:

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Initial Certification Date:

08 August 1996

Marc Bivona
Lead Auditor

Lack of fulfillment of conditions as set out in the Appendix may render this certificate invalid.

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- IMP International Sales Locations Listed by Country

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From San Francisco International Airport

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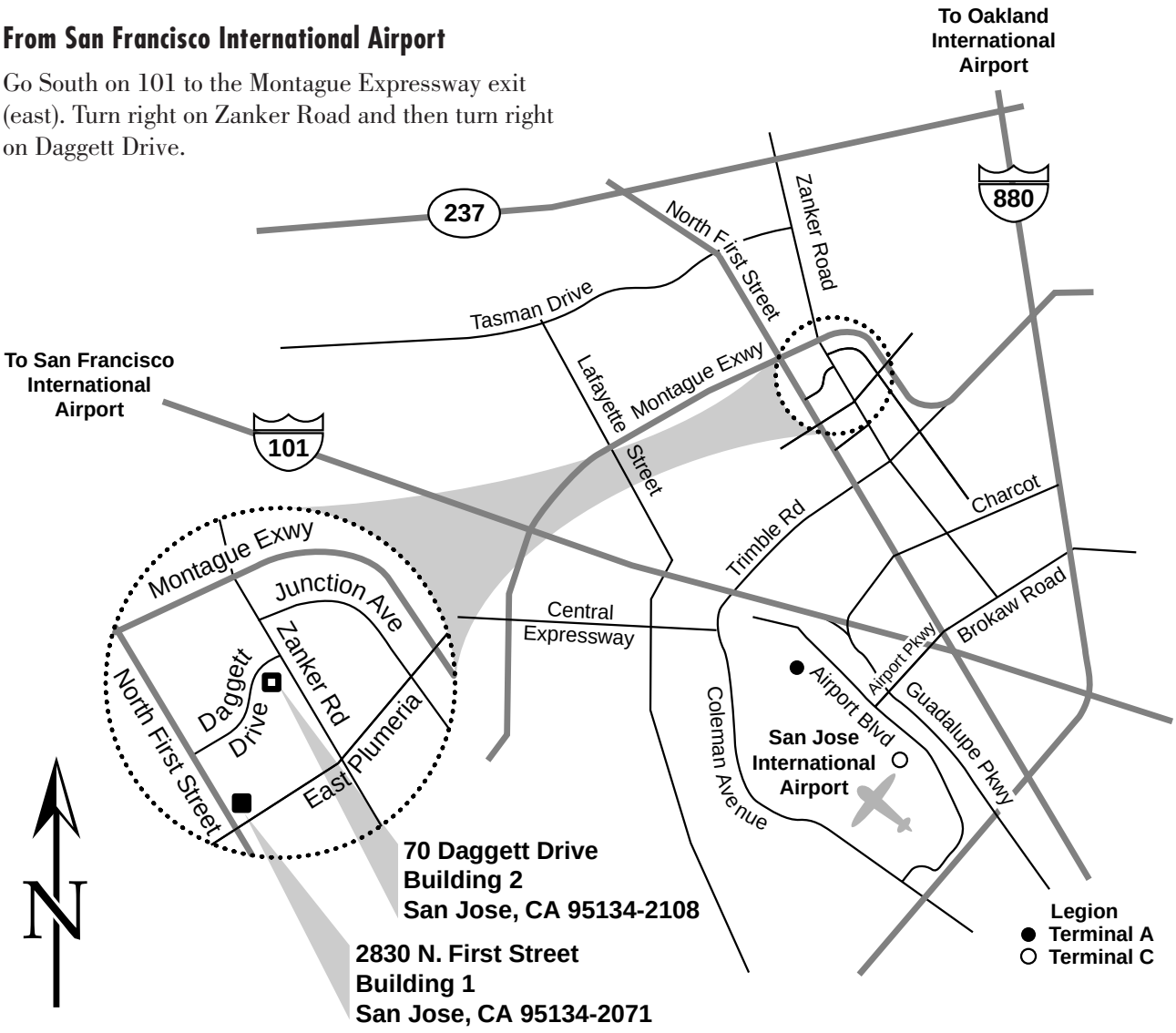

For Additional Directions

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	C0809	0.8	2	2	14	N		■										5		
◆	C0810	0.8	2	2	15	N		■					■					5		High Density Analog Circuits
	C1004	1.0	1	2	12	N	■											5		Gate Array Applications
	C1012	1.0	1	2	14	N												5		NCR Equivalent
	C1015	1.0	2	2	14	N		■										5		
◆	C1026	1.0	2	2	20	N		■	■		■			■	■	5		5	20	
◆	C1027	1.0	2	2	18	N		■	■		■			■		5		5	20	
◆	C1028	1.0	2	2	20	N		■	■		■			■		5		5	20	
◆	C1029	1.0	2	2	20	N		■	■		■		■		■	5		5	20	
	C1201	1.2	1	2	11	N	■											5		
	C1202	1.2	2	2	12	N		■										5		
	C1203	1.2	2	2	14	N			■							5		5		Low cost 2GHz Process
	C1206	1.2	2	2	16	N			■							5		5		6.4GHz Process
	C1209	1.2	2	2	14	N				■								5		Mixed-Signal Process
	C1210	1.2	2	2	14	N		■				■						5		Zero Threshold Devices
	C1212	1.2	2	2	17	N		■	■								12	5		
	C1215	1.2	2	2	13	N		■				■						5		Low Threshold Devices
	C1216	1.2	2	2	15	N		■			■								15	Under Development
	C1219	1.2	2	2	17	N		■		■		■	■					5		
	C1221	1.2	2	2	18	N		■	■				■			5		5		6.2GHz
	C1225	1.2	1	2	16	N		■	■							5		5		
	C1226	1.2	2	2	19	N		■			■							5	100	
	C1227	1.2	2	2	15	N		■	■		■		■			5			30	
◆	C1229	1.2	2	2	13	N		■			■		■					5	30	
◆	C1230	1.2	2	2	18	N		■	■					■		5		5		
◆	C1231	1.2	2	2	16	N		■	■		■			■		5	30	5	30	
◆	C1232	1.2	2	2	20	N		■	■	■		■	■			5		5		
	C1601	1.6	2	2	13	N		■										5		Mixed-Signal Designs
	C3013	3	2	1	11	P		■										5	10	
	C3014	2	2	1	10	P						■						5	10	
	C3015	3	1	1	9	P	■												10	
	C3017	3	2	2	13	P		■											10	
	C3025	3	2	1	9	P		■											10	
	C5014	5	2	1	11	P		■			■								15	15V RCA/AMI Equivalent

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